Vendor-Assisted Qualification/Vendor Self-Qualification Process and DRAM Qualification Test Procedure

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ABSTRACT: This specification describes the process used by Digital Equipment Corporation to perform vendor-assisted qualification (VAQ) and vendor self-qualification (VSQ) work on DRAMS.

APPLICABILITY: This specification is used by Digital personnel as a guide and reference document for qualification work, and it is used by Digital's DRAM suppliers to provide Digital with the information needed to perform VAQs and VSQs on DRAMS.

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CHAPTER 1

VENDOR–ASSISTED QUALIFICATION/VENDOR SELF-QUALIFICATION PROCESS FLOW

1.1 INTRODUCTION

This document describes the process used at Digital for performing vendor-assisted qualification work on DRAMs, for both first time qualifications (VAQ), and for re-qualifications (VSQ). It is used by Digital personnel as a guide and reference document for qualification work, and it is used by Digital's DRAM suppliers to supply Digital the information and data needed to perform VAQs and VSQs on DRAMs.

1.2 OVERVIEW

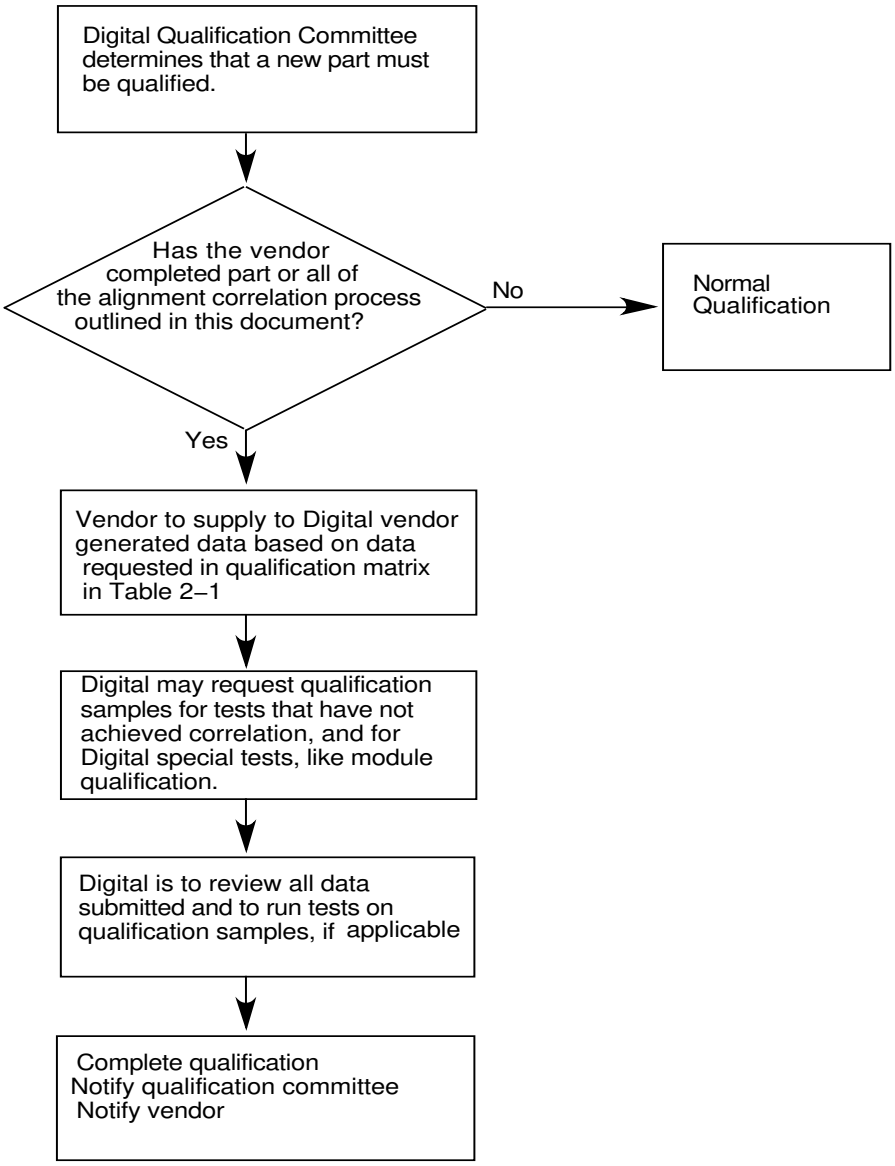
Figure 1-1 shows how Digital decides whether a qualification will be done vendor-assisted, or whether the normal qualification process will be used.

If vendor assisted, the qualification may be done using vendor-supplied data from one to three groups of tests. Use of vendor supplied data is determined by the results of a correlation study that must be successful for Digital to accept vendor data for each test. There may be certain tests that are not possible to correlate, for various reasons. In these cases, Digital may request qualification samples and will run the tests as needed.

Table 1-1 outlines the tests in each of the three groups. Group 1 tests are industry standard tests that require only a test process alignment and no correlation study. Groups 2 and 3 tests require both alignment and correlation for the vendor data to be used by Digital.

Table 1-2 summarizes the minimum qualification testing that will be performed for various changes in the DRAM that are made by the vendor. Following this table, the details of each qualification test done at Digital are described.

Figure 1–1: Vendor–Assisted Qualification (VAQ) Process Flow


Digital Qualification Committee determines that a new part must be qualified.
Has the vendor completed part or all of the alignment correlation process outlined in this document?
No
Normal Qualification
Yes
Vendor to supply to Digital vendor generated data based on data requested in qualification matrix in Table 2–1
Digital may request qualification samples for tests that have not achieved correlation, and for Digital special tests, like module qualification.
Digital is to review all data submitted and to run tests on qualification samples, if applicable
Complete qualification
Notify qualification committee
Notify vendor

NOTES FOR IMPLEMENTATION OF VAQ/VSQ PROCESS

1. **Digital reserves the right to request the vendor supply test samples with test data for any qualification test.**
2. **All tests are to be done on a sample containing parts from a minimum of three wafer lots and three packaging date codes.**

Table 1–1: Three Groups of Tests for Qualification

Group 1		
Autoclave	High Temperature Storage	
Temperature Cycling	Thermal Shock	85/85
Mechanical Shock	Plating Adhesion	Die Photo
X-Ray	Lead Integrity	Solderability
Visual/Mechanical		

Group 2		
Latch-Up	Thermal Resistance	HAST
Capacitance	Marking Permanence	Physical Dimensions
Plating Analysis	Coplanarity	

Group 3
Electrical Characterization (SHMOOs, IDD, Pattern Sens, Long Electrical)
HTOL
Process Compatibility
ESD
Hot Carrier

CHAPTER 2

DRAM QUALIFICATION MATRIX

The following matrix outlines the *minimum* testing required for common types of qualifications. Additional testing may be performed at the discretion of the responsible component engineer to ensure compliance with appropriate quality and reliability specifications.

Table 2–1: Qualifications

	TYPES OF QUALIFICATION (NOTE 6)							
Stress Test SS/Acc#	**DIE Re–design (Note 8)**	**DIE Shrink**	**FAB Loc/ Process Change**	**Assy Loc Change**	**New Package**	**Speed Sort**	**Test Process Change**	**Full Qual**
I. ELECTRICAL TESTS								
3.1 Production Test 231/0	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX				XXXXXXXX XXXXXXXX	XXXX XXXX
3.2 Pattern Sensitivity 22/0	Note 1 and Note 2	Note 2	XXXXXXXX XXXXXXXX	Note 2	Note 2		XXXXXXXX XXXXXXXX	Note 2
3.3 Electrical Char. 22/0	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX	Selected SHMOOs	XXXXXXXX XXXXXXXX	Selected SHMOOs	XXXX XXXX
3.4 SHMOOs 22/0								XXXX
3.5 IDD Peak 5/0	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX				XXXXXXXX XXXXXXXX		XXXX XXXX
3.6 ESD 10/0	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXXXXXX XXXXXXXX			XXXX XXXX
3.7 Capacitance 11/0	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXXXXXX XXXXXXXX			XXXX XXXX
3.8 Latch up 22/0	X CMOS X X only X	X CMOS X X only X						CMOS only

Table 2-1: Qualifications (continued)

	TYPES OF QUALIFICATION (NOTE 6)							
Stress Test SS/Acc#	DIE Re–design (Note 8)	DIE Shrink	FAB Loc Process Change	Assy Loc Change	New Package	Speed Sort	Test Process Change	Full Qual
II. MECHANICAL/ENVIRONMENTAL TESTS								
4.1 Physical Dimensions 11/0			XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX			XXXX XXXX
4.2 Solderability 45/0			XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX			XXXX XXXX
4.3 Lead Integrity 11/0					Non–SMD only			Non SMD
4.4 Autoclave 105/2					XXXXXXXX XXXXXXXX			XXXX XXXX
4.5 High Temperature–Storage 15/0					XXXXXXXX XXXXXXXX			XXXX XXXX
4.7 X–Ray 11/0	Note 7	XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXX XXXX
4.8 Visual/Mechanical 11/0				XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXX XXXX
4.9 Mark Permanence 11/0				XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXX XXXX
4.10 Plating Analysis 22/0					X SMD X X only X			SMD only
4.11 Temperature Cycle 15/0					XXXXXXXX XXXXXXXX			XXXX XXXX
4.12 Thermal Shock 11/0				XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXX XXXX
4.13 85/85 105/2					XXXXXXXX XXXXXXXX			XXXX XXXX
4.14 HAST 105/2					XXXXXXXX XXXXXXXX			XXXX XXXX
4.15 Mechanical Shock 11/0					Non–SMD only			Non SMD
4.16 Die Photo 1/NA	XXXXXXXX XXXXXXXX	XXXXXXXX XXXXXXXX			XXXXXXXX XXXXXXXX			XXXX XXXX
4.17 Co–Planarlty 76/0				X SMD X X only X	X SMD X X only X			SMD only
4.18 Plating Adhesion 5/0				X SMD X X only X	X SMD X X only X			SMD only
4.19 Process Compatibility 231/0				X SMD X X only X	X SMD X X only X			SMD only

Table 2-1: Qualifications (continued)

	TYPES OF QUALIFICATION (NOTE 6)							
Stress Test SS/Acc#	**DIE Re–design (Note 8)**	**DIE Shrink**	**FAB Loc/ Process Change**	**Assy Loc Change**	**New Package**	**Speed Sort**	**Test Process Change**	**Full Qual**
III. RELIABILITY TESTS								
5.1 Operational Test Det. by CE See 21–00006–GS	Note 1	XXXXXXXX XXXXXXXX			XXXXXXXX XXXXXXXX			XXXX XXXX
5.2 Hot Carrier 22/0	Note 1	XXXXXXXX XXXXXXXX						XXXX XXXX
5.3 Accelerated Life Test Det. by CE See 21–00006–GS	Note 1	XXXXXXXX XXXXXXXX	Note 5					XXXX XXXX
5.4 Module Qualification Det. by CE See 21–00006–GS	Note 1	XXXXXXXX XXXXXXXX			XXXXXXXX XXXXXXXX	Note 3		XXXX XXXX
Devices Needed	7500 max 1300 for bond opt	7500 max	2500 max	600	6000 max	4300 max	400	8000 max

Notes:

1. The responsible engineer will determine if this test will be done.
2. In this case, initial device test results from other qualification tests are used as data for reduced electeical test.
3. Speed sort is not generally required.
4. This test done for fab process qualifications only.
5. Qualification testing for assembly process changes will be determined on an individual basis.
6. X–Ray done for bonding option qualifications only.
7. These tests will also apply when evaluating metal mask and bonding options used to select the mode of operation or the input and outputr configuration.

CHAPTER 3

DRAM QUALIFICATION ELECTRICAL TEST PROCEDURES

3.1 DATALOG ROUTINE AND PRODUCTION TEST

The datalog routine is used to electrically test devices before and after environmental and physical stress, and to verify the functionally of the device per the Digital purchase specification. All operating modes are exercised using worst-case timing conditions, input and output levels, temperatures, and power supply values. To minimize test times, pattern sensitivity testing has not been included in the datalog routine.

Please note that the supplier is not under any obligation to duplicate Digital's test conditions since the supplier best understands the strengths and weaknesses of their particular device and can, therefore, develop the most efficient and comprehensive test process with respect to fault coverage. However, it is our expectation that whatever qualification test process the supplier uses, it will have at least the same, if not greater, fault coverage as specified in Digital's process. If the supplier has a more efficient production test process that guarantees the same amount of fault coverage (example: Test mode, RMW and VBUMP as a single test, and so forth), or if the conditions differ from Digital's specified process, the supplier must provide documentation of the test conditions for those particular tests.

The appropriate sample sizes for each test are listed in this document. Samples subjected to the following electrical tests must demonstrate a parts defect rate that is less than specified in Digital's A-PS-2100006-GS *DRAM General Quality Purchase Specification*. In the case of post environmental and physical stress, the sample must meet the LTPD as specified in Table 2-1.

If the responsible component engineer would like to expedite pre-environmental and post-environmental testing, he or she can decide to terminate the flow after completing conditions in 3.1.3.2. However, the same test flow should be used for both pre-testing and post-testing.

3.1.1 DC TESTS

This section outlines the dc tests done by Digital on DRAMs.

3.1.1.1 Input and Output Leakages

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
VIH = max
VIL = min
VCH = max

VCL = min

Method: Power up device, allow sufficient time for the power supply to stabilize, bias pins to their appropriate dc level, force voltage, and measure the associated leakage current on a pin-by-pin basis. The pin under test should be biased to the opposite logic state of the pins not being tested. Output leakage should be measured with the output(s) in a Hi-Z state. If the device uses CMOS output drivers, output leakage should be measured with VIH = VCC(max) + V(th).

Failure Criteria Device exceeds leakage current specification limit in the Digital purchase specification.

3.1.1.2 IDD Standby

This section outlines the IDD standby tests done by Digital on DRAMs.

3.1.1.2.1 TTL STBY Current

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
/R and /C = VCH min
All other pins = VCL/VIL max and/or VCH/VIH min
Outputs: Disconnected from load

Method: Power up device, pause for power supply to stabilize, execute minimum number of /R or CBR wake up cycles, bias input and output pins to their appropriate dc level, and measure IDD standby current.

Failure Criteria Device exceeds TTL IDD standby current specified limit in the Digital purchase specification.

3.1.1.2.2 CMOS STBY Current

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
/R and /C = VDD - V(th)
All other pins = VCL/VIL max and/or VCH/VIH min.
Outputs: Disconnected from load

Method: Power up device, pause for power supply to stabilize, execute minimum number of /R or CBR wake up cycles, bias input and output pins to their appropriate dc level, and measure CMOS IDD standby current.

Failure Criteria: Device exceeds CMOS IDD standby current specified limit in the Digital purchase specification.

3.1.1.2.3 TTL STBY Current with /R Deasserted and /C Asserted

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
/R = VCH min
/C = VCL max
All other pins = VIL/VCL max and/or VCH/VIH min
Outputs: Disconnected from the load

Method: Power up device, pause for power supply to stabilize, execute minimum number of /R or CBR wake up cycles, bias input and output pins to their appropriate dc level, and measure TTL IDD standby current.

Failure Criteria: Device exceeds IDD standby current specified limit in the Digital purchase specification.

3.1.1.2.4 CMOS STBY Current with /R Deasserted and /C Asserted

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
/R = VDD - V(TH)
/C = VSS
All other pins = VIL/VCL max and/or VCH/VIH min
Outputs: Disconnected from the load

Method: Power up device, pause for power supply to stabilize, execute minimum number of /R or CBR wake up cycles, bias input and output pins to their appropriate dc level, and measure CMOS IDD standby current.

Failure Criteria: Device exceeds IDD standby current specified limit in the Digital purchase specification.

3.1.2 AC TESTS

This section outlines the ac tests done by Digital on DRAMs.

3.1.2.1 IDD(ave) Active

This section outlines the IDD (ave) active tests done by Digital on DRAMs.

3.1.2.1.1 IDD(ave) Active, R/W Current

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
Cycle time = min tRC
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.

Data driver format: Surround by complement address
Data pattern: MarchX (see Section 3.2)
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR wake up cycles, write background, and while looping on a Read/Write (R/W) functional test (MarchX), measure the IDD(ave) R/W current.

Failure Criteria: Device exceeds the IDD(ave) active R/W current specified limit in the Digital purchase specification.

3.1.2.1.2 IDD(ave) Active, PMODE R/W

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
Cycle time = tPC min, tRAS/tCAS low time should be maximized.
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data driver format: Surround by complement
Address/data pattern: MarchY (see Section 3.2)
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR wake up cycles, write background and while looping on a PMODE R/W functional test (MarchY), measure the IDD(ave) PMODE current.

Failure Criteria: Device exceeds the IDD(ave) active PMODE current specified limit in the Digital purchase specification.

3.1.2.1.3 IDD(ave) Active, ROR Refresh

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
Cycle time = min tRC
VIH/VCH = min
VIL/VCL = max
Outputs:\bold) Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR wake up cycles, write background, and while looping on a ROR functional test, measure the IDD(ave) ROR current.

Failure Criteria: Device exceeds the IDD(ave) active ROR current specified limit in the Digital purchase specification.

3.1.2.1.4 IDD(ave) Active, CBR Refresh

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
Cycle time = min tRC
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR wake up cycles, write background, and while looping on a CBR functional test measure the IDD(ave) CBR current.

Failure Criteria: Device exceeds the IDD(ave) active CBR current specified limit in the Digital purchase specification.

3.1.2.1.5 IDD(ave) Active, TMODE

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
Cycle time = min tTRC
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data driver format: Surround by complement
Address/data pattern: MarchX (see Section 3.2)
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR wake up cycles, execute test mode entry cycle, write background, and while looping on a R/W functional test measure the IDD(ave) R/W TMODE current.

Failure Criteria: Device exceeds the IDD(ave) active test mode R/W current specified limit in the Digital purchase specification.

3.1.2.1.6 IDD(ave) Active, Full Read Data Transfer with Serial Port Inactive

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
RAM Cycle time = min tRC
SAM Cycle time = /SE deasserted/asserted, SC held high or low
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted

Data driver format: Surround by complement
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR and SC wake up cycles, write background, and while looping on full read data transfer cycles with the serial port inactive, measure the IDD(ave) current.

Failure Criteria: Device exceeds the IDD(ave) active full read data transfer current specification limit in the Digital purchase specification.

3.1.2.1.7 IDD(ave) Active, Full Write Data Transfer with Serial Port Inactive

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
RAM Cycle time = min tRC.
SAM Cycle time = SC held high or low.
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data driver format: Surround by complement
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR and SC wake up cycles, write background, execute a full read data transfer cycle followed by a pseudo or a masked write transfer cycle, and while looping on full write data transfer cycles with the serial port inactive, measure the IDD(ave) current.

Failure Criteria: Device exceeds the IDD(ave) active full write data transfer current specification limit in the Digital purchase specification.

3.1.2.1.8 IDD(ave) Active, Split Read Transfer with Serial Port Inactive

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
RAM Cycle time = tRC min
SAM Cycle time = /SE deasserted, SC held high or low
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data driver format: Surround by complement
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR and SC wake up cycles, write background, execute a full read data transfer cycle, and while looping on split read data transfer cycles with the serial port inactive, measure the IDD(ave) current.

Failure Criteria: Device exceeds the IDD(ave) active split read transfer current specified limit in the Digital purchase specification.

3.1.2.1.9 IDD(ave) Active, RAM and Serial Port Active

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
RAM Cycle time = tRC min
SAM Cycle time = tSCC min
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices.
Address: Single address transition with /RAS asserted and /CAS deasserted.
Data driver format: Surround by complement
Address/data pattern: Address scan (see Section 3.2), Ckbd/inv-ckbd
Address/data topologies: Enabled

Method: Power up device, pause for power supply to stabilize, execute /R or CBR and SC wake up cycles, write background, execute a full read data transfer cycle and while looping on a RAM R/W functional test (Address scan) with the serial port active, measure the IDD(ave) current.

Failure Criteria: Device exceeds the IDD(ave) active RAM/SAM port current specified limit in the Digital purchase specification.

3.1.2.1.10 IDD(ave) Active, Serial Port Active with RAM Port Inactive

Conditions:

Temperature = min/typ/max, operating
VDD = max, operating
RAM Cycle time = /RAS and /CAS deasserted except for a refresh cycle every tREF/(number of rows)
SAM Cycle time = tSCC min
VIH/VCH = min
VIL/VCL = max
Outputs: Disconnected from the load, outputs tristated for common I/O devices
Data driver format: Surround by complement
Data pattern: Ckbd/inv-ckbd
Address/data topologies: Optional

Method: Power up device, pause for power supply to stabilize, execute /R or CBR and SC wake up cycles, write background, execute a full read data transfer cycle and while looping with the RAM port inactive and the serial port active, measure the IDD(ave) current.

Failure Criteria: Device exceeds IDD(ave) active SAM current specified limit in the Digital purchase specification.

3.1.3 FUNCTIONAL OPERATION

3.1.3.1 R/W Operation @ Min tRCD/tRAD

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tRC min, early write operation
tRCD/tRAD = min
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address drivers format: Row to column
Data driver format: Surround by complement
Address/data pattern: Address scan (see Section 3.2), Ckbd/inv-ckb
Address/data topologies: Optional
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight R/W timing conditions.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.2 R/W Operation @ Max tRCD/tRAD

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tRC min, late write operation
tRCD/tRAD = max
VIL/VCL = min
VIH/VCH = max
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: MarchY
Address/data topologies: Optional
Refresh enabled: Yes, CBR burst
Rise/Fall times: 8ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight R/W timing conditions.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.3 RMW Short Cycle

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
cycle = tRWC min
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: MarchX (see Section 3.2)
Address/data topologies: Optional
Refresh enabled: No
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight RMW timing conditions.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.4 RMW Long Cycle

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tRWC max, tRAS/tCAS max
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: Address scan (see Section 3.2), Ckbd/ inv-ckbd
Address/data topologies: Optional
Refresh enabled: Yes, CBR burst
Rise/Fall times: 2ns
Strobe: Long window
Load conditions: Per Digital specification

Method: Exercise device using long tRAS RMW timing conditions. Strobe for data at access time and maintain strobe until write operation occurs at very end of cycle.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.5 PMODE R/W Cycle

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
cycle = tPC min, early write operation
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: MarchY (see Section 3.2)
Address/data topologies: Optional
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight PMODE R/W timing conditions.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.6 PMODE RMW Cycle

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tPRWC min, maximize tRAS/tCAS low time
tRCD/tRAD = min
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Row to column for entry cycle, SBC during PMODE
Data driver format: Surround by complement
Address/data pattern: MarchY (see Section 3.2)
Address/data topologies: Optional
Refresh enabled: Yes, CBR burst
Rise/Fall times: 2ns
Strobe: Window

Load conditions: Per Digital specification

Method: Exercise device using tight PMODE RMW timing conditions.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.7 VBUMP

Conditions:

Temperature = min/typ/max, operating
VDD = VDD(min) to VDD(min) + VBUMP, VDD(min) + VBUMP to VDD(min)
VDD(max) to VDD(max)- VBUMP, VDD(max) - VBUMP to VDD(max)
Cycle = tRC min, late write operation
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: MarchX (see Section 3.2)
Address/data topologies: Optional
Refresh enabled: No
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight R/W timing conditions while bumping power supply between VDD(min) and VDD(max).

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.8 Test Mode Check

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tTRC min, early write operation
tRCD/tRAD = min
VIL/VCL = min
VIH/VCH = max
VOL = max
VOH = min
IOL/IOH = max
Address drivers format: Row to column
Data driver format: Surround by complement
Address/data pattern: MarchY (see Section 3.2)
Address/data topologies: Optional

Refresh enabled: Yes, CBR distributed, with WE asserted
Rise/Fall times: 8ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight R/W timing conditions with test mode enabled.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.9 HIDDEN Refresh

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tRC min, early write operation
tRCD/tRAD = min
VIL/VCL = min
VIH/VCH = max
VOL = max
VOH = min
IOL/IOH = max
Address drivers format: Row to column
Data driver format: Surround by complement
Address/data pattern: MarchY (see Section 3.2)
Address/data topologies: Optional
Refresh enabled: Yes, hidden refresh
Rise/Fall times: 8ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight HIDDEN REFRESH timing conditions. Execute hidden refresh cycles during read and write cycles. For read cycles maintain data strobe until /CAS is deasserted.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.10 R/W Write Per Bit Test

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tRC min, late write operation
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement

Data driver format: Surround by complement
Address/Data pattern: Address scan (see Section 3.2), Ckbd/inv-ckbd
Address/data topologies: Optional
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight R/W timing conditions with WPB enabled. All I/O mask combinations should be exercised.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.11 PMODE Write Per Bit Test

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle = tPC min, early write operation
tRCD/tRAD = min
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: MarchY (See Section 3.2)
Address/data topologies: Optional
Refresh enabled: Yes, CBR distributed
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using tight PMODE timing conditions with WPB enabled. All I/O mask combinations should be exercised.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.12 Real Time Read Data Transfer Operation

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle time = tRC/tSCC min
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min

IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: Address scan (see Section 3.2), Ckbd/inv-ckbd and diagonal /inv-diagonal
Address/data topologies: Disabled
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Exercise device using real time read transfer timing conditions (RAM port serial port active). Exercise tap address from minimum to maximum.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.13 Write Data Transfer Operation

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle time = tRC/tSCC min
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: Address scan (See Section 3.2), Ckbd/inv-ckbd, and diagonal /inv-diagonal
Address/data topologies: Disabled
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Strobe: Window
Load conditions: Per Digital specification

Method: Functionally exercise device by clocking data into the serial register and executing a write data transfer operation. Fully exercise tap address. Read contents of DRAM after filling RAM with data from serial port.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.1.3.14 Split Register Read Data Transfer Operation

Conditions:

Temperature = min/typ/max, operating
VDD = min/max, operating
Cycle time = tRC/tSCC min
tRCD/tRAD = max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address driver format: Surround by complement
Data driver format: Surround by complement
Address/data pattern: Address scan (see Section 3.2), Ckbd/inv-ckbd, diagonal /inv-diagonal
Address/data topologies: Disabled
Refresh enabled: Yes, CBR distributed
Rise/Fall times: 2ns
Load conditions: Per Digital specification

Method: Exercise device using split read transfer timing conditions (RAM port, serial port active). Exercise tap address from minimum to maximum SC cycle count when split transfer cycle occurs should vary between minimum and maximum values.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.2 PATTERN SENSITIVITY

Pattern sensitivity testing verifies the device is not sensitive to any data or address sequences over all ranges and combinations of applied operating conditions.

Considering the intent of pattern sensitivity testing and test time limitations, exercising the device using tight-timing conditions and every operating mode is not mandatory. However, the device must accept, retain, and reproduce data without regard to the sequence or pattern of data, addresses, timing, and cycle types.

Please note that the supplier is not under any obligation to duplicate Digital's test conditions. If the supplier has a more efficient production test process that guarantees the same amount of fault coverage, the supplier should provide a description of the test conditions for Digital's review.

The sample size required for pattern sensitivity is listed in Table 2-1. Samples subjected to the following electrically tests must demonstrate a ppm defect rate that is less than what is specified in Digital's A-PS-2100006-GS *DRAM General Quality Purchase Specification.*

3.2.1 TEST CONDITIONS FOR PATTERN SENSITIVITY

Temperature = min/max, operating.
VDD = min/max, operating.
tRCD/tRAD = min/max
VIL/VCL = max
VIH/VCH = min
VOL = max
VOH = min
IOL/IOH = max
Address drivers format: Surround by complement
Data driver format: Surround by complement
Address/data topologies: Enabled
Refresh: CBR refresh distributed unless specified otherwise.
Rise/Fall times: 2ns
Load: Per Digital specification

Method: Exercise device using addressing/data sequences provided in Chapter 3, subheads 3.2.2.1 through 3.2.2.11.

Failure Criteria: Device fails to operate over all ranges and combinations of applied operating conditions.

3.2.2 ADDRESS AND DATA SEQUENCES

This section describes the address of data sequences used in Digital's DRAM test process.

3.2.2.1 MarchX

The flow for MarchX is as follows:

a. Write entire memory array with normal data.
b. At row address = 0, column address = 0, read normal data, write inverted data.
c. Increment row address, read normal data, write inverted data.
d. Repeat step c until row address = max, column address = max.
e. At row address = max, column address = max, read inverted data, write normal data.
f. Decrement row address, read inverted data, write normal data.
g. Repeat step f until row address = 0, column address = 0.
h. At row address = 0, column address = 0, read normal data.
i. Increment row address, read normal data.
j. Repeat step i until row address = max, column address = max.
k. Repeat steps a through j with opposite data.

3.2.2.2 MarchY

The flow for MarchY is as follows:

a. Write entire memory array with normal data.

b. At row address = 0, column address = 0, read normal data, write inverted data.

c. Increment column address, read normal data, write inverted data.

d. Repeat step c until row address = max, column address = max.

e. At row address = max, column address = max, read inverted data, write normal data.

f. Decrement column address, read inverted data, write normal data.

g. Repeat step f until row address = 0, column address = 0.

h. At row address = 0, column address = 0, read normal data.

i. Increment column address, read normal data.

j. Repeat step i until row address = max, column address = max.

k. Repeat steps a through j with opposite data.

3.2.2.3 Scanning Column Cell Float (Modified)

The flow for scanning column cell float is as follows:

a. Write entire memory array with normal data.

b. At row address = 0, column address = 0 (Target), read normal data, write inverted data, read inverted data, write normal data.

c. Increment column address, read normal data, write inverted data, read inverted data, write normal data.

d. At target address, read normal data, write inverted data, read inverted data, write normal data.

e. Repeat steps c through d until col address = max.

f. Increment target row address, set col address = 0, read normal data, write inverted data, read inverted data, write normal data.

g. Repeat steps c through f until row address = max, column address = max.

h. Repeat steps a through g with opposite data.

3.2.2.4 Moving Inversion

The flow for moving inversion is as follows:

a. Write entire array with normal data.

b. At row address = 0, column address = 0, read normal data, write inverted data, read inverted data.

c. Increment row address by 2**N (where N = 0 to maximum number of row address bits) and read normal data, write inverted data, read inverted data.

d. Repeat step c until row address = max, column address = max.

e. Set row address = 0, column address = 0, read inverted data, write normal data, read normal data.

f. Increment row address by 2**N (where N = 0 to maximum number of row address bits) and read inverted data, write normal data, read normal data.

g. Repeat step f until row address = max and column address = max.

h. At row address = max, column address = max, read normal data, write inverted data, read inverted data.

i. Decrement row address by 2**N (where N = 0 to maximum number of row address bits) and read normal data, write inverted data, read inverted data.

j. Repeat step i until row address = 0, column address = 0.

k. At row address = max, column address = max; read inverted data, write normal data data, read normal data.

l. Decrement row address by 2**N (where N = 0 to maximum number of row address bits) and read inverted data, write normal data, read normal data.

m. Repeat step l until row address = 0 and column address = 0.

n. Increment N and repeat steps b through m where N = 0 to maximum number of row address bits.

o. Repeat steps b through n incrementing the column address by 2**N instead of the row address where N = 0 to maximum number of column address bits.

3.2.2.5 Adjacent Row Disturb

The flow for adjacent row disturb is as follows:

a. Write entire memory array with normal data.

b. At row address = 1, column address = 0, write inverted data.

c. Increment column address, write inverted data, inhibit address carries from column to row.

d. Repeat step c until tREF = tREF(max)

e. Set column address = 0, decrement row address, read normal data.

f. Increment column address, read normal data.

g. Repeat step f until column address = max.

h. Refresh entire array.

i. Set column address = 0, increment row address, read inverted data, write normal data.

j. Increment column address, read inverted data, write normal data.

k. Repeat step j until column address = max.

l. Set column address = 0, increment row address, read normal data.

m. Increment column address, read normal data.

n. Repeat step m until column address = max.

o. Set column address = 0, write inverted data.

p. Repeat steps c through o until row address = max, column address = max.

q. Repeat steps a through r with opposite data.

3.2.2.6 Adjacent Column Disturb

The flow for adjacent column disturb is as follows:

a. Write entire memory array with normal data.
b. At row address = 0, column address = 1, write inverted data.
c. Increment row address, write inverted data, inhibit address carries from row to column.
d. Repeat step c until tREF = tREF(max)
e. Set row address = 0, decrement column address, read normal data.
f. Increment row address, read normal data.
g. Repeat step f until row address = max.
h. Refresh entire array.
i. Set row address = 0, increment column address, read inverted data, write normal data.
j. Increment row address, read inverted data, write normal data.
k. Repeat step j until row address = max.
l. Set row address = 0, increment column address, read normal data.
m. Increment row address, read normal data.
n. Repeat step m until row address = max.
o. Set row address = 0, write inverted data.
p. Repeat steps c through o until row address = max, column address = max.
q. Repeat steps a through r with opposite data.

3.2.2.7 Surround Disturb

The flow for surround disturb is as follows:

a. Write entire array with normal data.
b. At row address = 0, column address = 0 (Target); read normal data, write inverted.
c. Increment column address, read normal data, write inverted data, read inverted data, write normal data, read normal data.
d. Increment row address; read normal data, write inverted data, read inverted data, write normal data, read normal data.
e. Decrement column address; read normal data, write inverted data, read inverted data, write normal data, read normal data.
f. Decrement column address; read normal data, write inverted data, read inverted data, write normal data, read normal data.
g. Decrement row address; read normal data, write inverted data, read inverted data, write normal data, read normal data.
h. Decrement row address; read normal data, write inverted data, read inverted data, write normal data, read normal data.
i. Increment column address; read normal data, write inverted data, read inverted data, write normal data, read normal data.

j. Increment column address; read normal data, write inverted data, read inverted data, write normal data, read normal data.

k. Read target cell and write target cell back to normal data.

l. Increment row address of target cell and repeat steps c through k until row address = max and column address = max.

m. Repeat steps a through l with opposite data.

3.2.2.8 Stall

The flow for stall is as follows:

a. Write entire array with normal data.

b. Pause for tREF.

c. Execute minimum number of refresh cycles to refresh entire device.

d. Repeat steps b through c 1024 times.

e. Read entire array.

f. Repeat steps a through e with opposite data.

3.2.2.9 Address scan and Address/Address Complement

The flow for address scan and address complement is as follows:

a. Write entire array with normal data.

b. Read and write entire array using the following addressing sequences (minimum to maximum x-fast, minimum to maximum x-fast, address/address complement x-fast, minimum to maximum y-fast, max to min y-fast, address/address complement y-fast).

c. Repeat step b with opposite data.

d. Repeat steps a through c using the following data patterns (ckbd, horizontal/vertical stripes, sliding diagonal)

3.2.2.10 Sliding Bit Test for xN I/O Devices

The flow for sliding bit test for xN I/O devices (x4 as an example, is as follows:

a. Write entire memory array with sliding bit pattern (that is, at address (0,0) write 0001, at address (1,0) write 0010, at address (2,0) write 0100, and so on)

b. Read entire array (minimum to maximum x-fast, minimum to maximum x-fast, minimum to maximum y-fast, minimum to maximum y-fast, address/address complement x-fast, address/address complement y-fast)

c. Repeat steps a through c with opposite data.

3.2.2.11 Row Galpat (modified)

The flow for row galpat is as follows:

a. Write entire memory array with normal data

b. At row address = 0, column address = 0 (Target), read normal data, write inverted data, read inverted data, write normal data.

c. Increment row address, read normal data, write inverted data, read inverted data, write normal data.

d. At target address, read normal data, write inverted data, read inverted data, write normal data.

e. Repeat steps c through d until row address = max.

f. Increment target column address, set row address = 0, read normal data, write inverted data, read inverted data, write normal data.

g. Repeat steps c through f until row address = max, column address = max.

h. Repeat steps a through g with opposite data.

3.3 CHARACTERIZATION

The characterization routine provides the electrical margin to a specific parameter, or if a failure is encountered, which parameter(s) is(are) the cause of the failure(s). Parameters that are simple summations of other parameters do not have to be characterized.

Please note that the supplier is not under any obligation to duplicate Digital's test conditions. If the supplier has a more efficient production test process that guarantees the same amount of fault coverage, the supplier should provide a description of the test conditions for Digital's review.

The sample size required for characterization is listed in Table 2-1. Samples subjected to the following electrical tests must demonstrate a ppm defect rate that is less than what is specified in Digital's A-PS-2100006-GS *DRAM General Quality Purchase Specification.*

3.3.1 TEST CONDITIONS FOR CHARACTERIZATION

Temperature = min/nom/max, operating
VDD = min/nom/max, operating
VIL/VCL = nominal
VIH/VCH = nominal
VOL = max
VOH = min
IOL/IOH = max
Data driver format: Surround by complement
Address/data topologies: Optional
Timing: Loose except for the parameter under test.
Rise/Fall times: 2ns
Load Conditions: Per Digital specification
Failure Criteria: Characterized parameter exceeds value specified in the Digital purchase specification.

3.3.2 PARAMETERS TO BE CHARACTERIZED

Parameters to be characterized along with their addressing and patterns are as follows:

3.3.2.1 VIH/VIL/VCH/VCL

Parameter: Input levels
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.2 VOH/VOL

Parameter: Output levels
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.3 IDD(n)

Parameters: IDD(ave) active
Addressing/pattern: Address scan (see Section 3.2)
Operating modes: R/W, CBR, ROR, PMODE, R/W data transfer operations with serial port active/inactive.
Timing: Single and multiple address transitions while RAS=VCL and CAS=VCH.

3.3.2.4 tRAS

This section describes tRAS characteristics along with the addressing and patterns.

3.3.2.4.1 tRAS (min)

Parameter: Min /RAS pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD

3.3.2.4.2 tRAS (max)

Parameter: Max /RAS pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read modify write

3.3.2.4.3 tRAS (max)

Parameter: Max /RAS pulse width
Addressing/pattern: MarchY (see Section 3.2)
Operating mode: Page Mode

3.3.2.5 tCAS

This section describes tCAS characteristics along with the addressing and patterns.

3.3.2.5.1 tCAS (min)

Parameter: Min /CAS pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ max tRCD/tRAD.

3.3.2.5.2 tCAS (max)

Parameter: Max /CAS pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read modify write

3.3.2.6 tRP

Parameter: /RAS precharge time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Page Mode

3.3.2.7 tASR

Parameter: Row address setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD.

3.3.2.8 tRAH

Parameter: Row address hold time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD.

3.3.2.9 tASC

Parameter: Column address setup time
Addressing/pattern: Address scan (see Secton 3.2)
Operating mode: R/W @ max tRCD/tRAD.

3.3.2.10 tCAH

Parameter: Column address hold time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ max tRCD/tRAD

3.3.2.11 tREF

This section describes tREF characteristics along with the addressing and patterns.

3.3.2.11.1 tREF(1)

Parameter: Refresh period
Addressing/pattern: Stall (see Section 3.2)
Operating mode: R/W with CBR burst refresh

3.3.2.11.2 tREF(2)

Parameter: Refresh period
Addressing/pattern: MarchY (see Section 3.2)
Operating mode: R/W with distributed CBR refresh

3.3.2.12 tRAC

Parameter: /RAS access time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD

3.3.2.13 tCAC

Parameter: /CAS access time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ max tRCD/tRAD

3.3.2.14 tCAA

Parameter: Column address access time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ max tRCD/tRAD

3.3.2.15 tOAC

Parameter: /OE access time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ max tRCD/tRAD

3.3.2.16 tCPA

Parameter: Access time from /CAS precharge
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: Page Mode R/W

3.3.2.17 tAR

Parameter: Column address hold time referenced to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD.

3.3.2.18 tRCS

Parameter: Read command setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.19 tOFF

This section describes tOFF characteristics along with the addressing and patterns.

3.3.2.19.1 tOFF(C)

Parameter: Output turnoff from /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.19.2 tOFF(OE)

Parameter: Output turnoff from /OE
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.20 tRCH

Parameter: Read hold time referenced to /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.21 tRRH

Parameter: Read hold time referenced to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.22 tWCS

Parameter: Write setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write

3.3.2.23 tWCH

Parameter: Write command hold time referenced to /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD

3.3.2.24 tWCR

Parameter: Write command hold time referenced to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ min tRCD/tRAD

3.3.2.25 tDS

This section describes tDS characteristics along with the addressing and patterns.

3.3.2.25.1 TDS(C)

Parameter: Data in setup referenced to /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/early write @ min tRCD/tRAD.

3.3.2.25.2 TDS(W)

Parameter: Data in setup referenced to /WE
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD.

3.3.2.26 tWP

Parameter: /WE pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD.

3.3.2.27 tCWL

Parameter: /WE lead time referenced /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD.

3.3.2.28 tRWL

Parameter: /WE lead time referenced to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD

3.3.2.29 tDH

This section describes tDH characteristics along with the addressing and patterns.

3.3.2.29.1 tDH(C)

Parameter: Data in hold time referenced to /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/early write @ max tRCD/tRAD

3.3.2.29.2 tDH(W)

Parameter: Data in hold time referenced to /WE
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read/late write @ max tRCD/tRAD

3.3.2.30 tDHR

Parameter: Data hold time referenced to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W @ min tRCD/tRAD

3.3.2.31 tCSR

Parameter: /CAS setup time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: CBR

3.3.2.32 tCHR

Parameter: /CAS hold time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: CBR

3.3.2.33 tCPN

Parameter: /CAS precharge
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: R/W

3.3.2.34 tWRP

Parameter: /WE to /RAS precharge time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: CBR

3.3.2.35 tWRH

Parameter: /WE to /RAS hold time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: CBR

3.3.2.36 tRPC

Parameter: /RAS precharge to /CAS hold time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: R/W

3.3.2.37 tCP

Parameter: /CAS precharge
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: PMODE

3.3.2.38 Write Per Bit Parameters

This section describes write per bit parameters.

3.3.2.38.1 tWBS

Parameter: Write per bit setup time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.38.2 tWBH

Parameter: Write per bit hold time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.38.3 tWDS

Parameter: Write per bit selection setup time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.38.4 tWDH

Parameter: Write per bit selection hold time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.39 VRAM Parameters

This section describes VRAM Parameters.

3.3.2.39.1 TSCA

Parameter: Access time from SC
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read data transfer/serial read

3.3.2.39.2 tSEA

Parameter: Access time from /SE
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read data transfer/serial read

3.3.2.39.3 tSEZ

Parameter: Serial output turnoff time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read data transfer/serial read

3.3.2.39.4 tSOH

Parameter: Serial output hold time from SC
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read data transfer/serial read

3.3.2.39.5 VOH/VOL

Parameter: Serial output levels
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Read data transfer/serial read

3.3.2.39.6 tDTS

Parameter: /DT to /RAS setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.7 tDTH

Parameter: /DT hold time relative to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.8 tESR

Parameter: /SE to /RAS setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.9 tREH

Parameter: /SE hold time relative to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.10 tRTH

Parameter: /DT hold time relative to /RAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Real time data transfer operation

3.3.2.39.11 tCTH

Parameter: /DT hold time relative to /CAS
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Real time data transfer operation

3.3.2.39.12 tTP

Parameter: /DT precharge time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.13 tRSD

Parameter: /RAS to first SC time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.14 tCSD

Parameter: /CAS to first SC time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.15 tTSL

Parameter: Last SC to /DT lead time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Real time data transfer operation

3.3.2.39.16 tTSD

Parameter: /DT to first SC delay time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Data transfer operation

3.3.2.39.17 tSRS

Parameter: Last SC to /RAS setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.18 tSRD

Parameter: /RAS to first SC delay time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.19 tSDD

Parameter: /RAS to serial input delay time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.20 tSC

Parameter: SC high pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.21 tSCP

Parameter: SC low pulse width
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.22 tSDS

Parameter: Serial input setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.23 tSDH

Parameter: Serial input hold time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.24 tSWS

Parameter: Serial write enable setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.25 tSEH

Parameter: Serial write enable hold time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.26 tSWIS

Parameter: Serial write disable setup time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.27 tSWIH

Parameter: Serial write disable hold time.
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.28 tSZS

Parameter: Serial input to first SC delay time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Serial R/W

3.3.2.39.29 tSDZ

Parameter: Serial output turnoff time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: Pseudo write transfer operation

3.3.2.39.30 tCRP

Parameter: /CAS to /RAS precharge time
Addressing/pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.3.2.39.31 tROH

Parameter: /RAS hold time referenced to /OE
Addressing/pattern: Address scan (see Section 3.2)

3.4 SHMOOS

SHMOOs verify the operation of the device over a wide range of voltage and timing conditions. In particular, holes within the device operating range are easily identified.

Please note that the supplier is not under any obligation to duplicate Digital's test conditions. If the supplier has a more efficient test process that guarantees the same amount of fault coverage, the supplier should provide a description of the test conditions for Digital's review.

The sample size required for SHMOOs is listed in Table 2-1. Samples subjected to the following tests must demonstrate a ppm defect rate that is less than what is specified in Digital's A-PS-2100006-GS *DRAM General Quality Purchase Specification.*

3.4.1 TEST CONDITIONS FOR SHMOO ROUTINES

VDD = VDD(nominal) ± 20%
Temperature = min/nom/max, operating
VIL/VCL = nominal
VIH/VCH = nominal
VOL = max
VOH = min
IOL/IOH = max
Address/Data driver format: Surround by complement
Address/data topologies: Optional
Timing: Loose except for the parameter under test.
Rise/Fall times: 2ns
Load: Per Digital specification

3.4.2 PARAMETERS TO BE SHMOOED

Following is a list of parameters to be SHMOOed.

3.4.2.1 VIL/VIH/VCL/VCH

Parameter: Input levels
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.4.2.2 VOL/VOH

Parameter: Output levels
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read

3.4.2.3 tRAC

Parameter: /RAS access time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read

3.4.2.4 tCAC

Parameter: /CAS access time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read

3.4.2.5 tCAA

Parameter: Column address access time
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: Read

3.4.2.6 tCPA

Parameter: /CAS precharge access time
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: Page Mode Read

3.4.2.7 tOEA

Parameter: Access time from /OE
Address/Pattern: NA
Operating mode: Read

3.4.2.8 tRP

Parameter: /RAS precharge
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: PMODE RMW

3.4.2.9 tREF

Parameter: Refresh period
Addressing/Pattern: MarchY (see Section 3.2)
Operating mode: R/W, burst, and distributed refresh

3.4.2.10 tRCD/tRAD

Parameter: /RAS to /CAS delay, RAS to column address delay
Addressing/Pattern: Address scan (see Section 3.2)
Operating mode: R/W

3.5 TEST—IDD8 R/W PEAK CURRENT PROCEDURE

Test IDD8 under the following general conditions:

All pins: Vih=2.4 V, Vil=0.8 V

Compare levels: Voh=2.4 V, Vol=400 mV Iol,Ioh=spec. max.

Vdd = 5.5 V

Temperature=0°C

Formatting:

Address: Surround by complement, both row and column address, tight setup and hold timing.

/RAS, /CAS, /WE: Return-to-one

DIN: Surround true data by complement data, with tight setup/hold timing.

Strobe: Window

Timing: Diagram 3-1

Special conditions:

Make sure current probe of adequate bandwidth is used.

Or a voltage probe across a 1-ohm resistor may be used.

While looping on a fast functional test, MarchX pattern, connect a current probe to the Vdd line on the load board. Connect another input of the oscilloscope to the RAS signal. Bring the device to 0°C, and photograph the current waveform. Clearly label the photograph of all units and divisions, signal name, Vdd, and so on.

Sample Size	5
Accept Number	0
Reject Criteria	Any device that draws more than the specified Idd8 current under these conditions shall be rejected.
VAQ/VSQ Data Required	Measured results on the sample devices.

3.6 TEST — ELECTROSTATIC DISCHARGE PROCEDURE

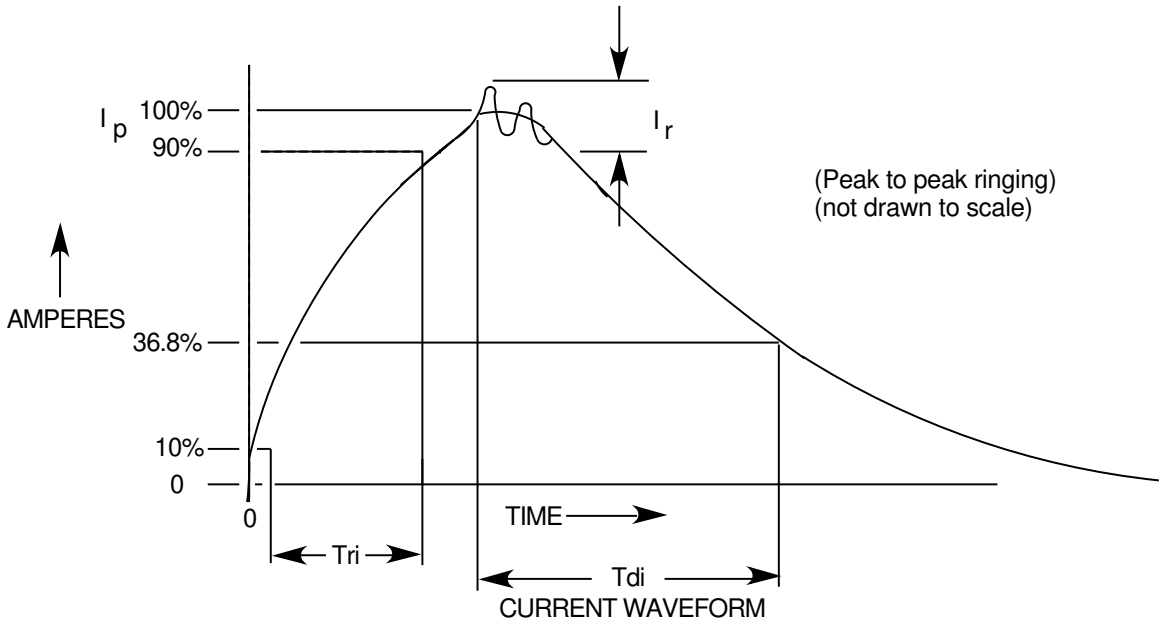
3.6.1 PURPOSE

This document defines the test methods and procedures to perform Electrostatic Discharge Testing.

3.6.2 EQUIPMENT

The equipment used should be capable of supplying the waveform shown in Figure 3–1 to the pin under test.)

Figure 3–1: Pin Under Test Waveform (Human Body Model)

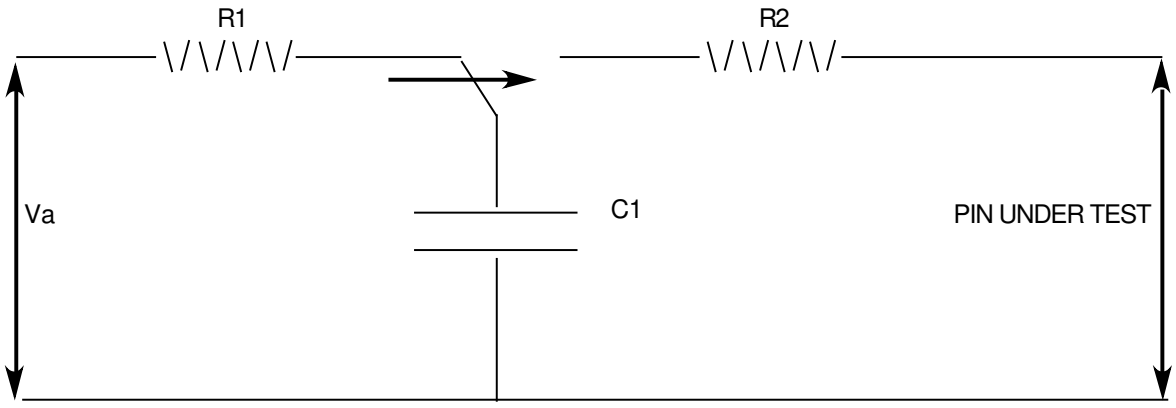


Notes:

The current pulse shall have the following charateristics:

Tri (rise time)	Less than 10 nanoseconds.
Tdi (delay time)	150 ± 20 nanoseconds.
I_p (peak current)	0.4 amperes, ±10%.
I_r (ringing)	The decay shall be smooth, with ringing, break points, double time constants or discountinuities less than 15 percent I_p maximum, but not observable 100 nanoseconds after start of the pulse.

The waveform, shown in Figure 3.1, may be produced by employing the following RC circuit along with the use of a regulated high voltage power supply.



R1 = 1000M Ohm min, current limiting resistor
R2 = 1500 Ohm ± 1%
C1 = 100pFI 10%
Va = Programmable Regulated High Voltage Power Supplly

3.6.3 CALIBRATION

Calibration of the test setup shall be performed by replacing the pin under test with a short circuit. The waveform that is to be calibrated is measured by using a current probe to measure the current going through the short circuit at the (PUT) terminals.

To properly measure the calibration current waveform, the oscilloscope and amplifier combination shall have a 350 MHz minimum bandwidth and a minimum 4 cm/ns visual writing speed. The current probe shall have a minimum bandwidth of 350 MHz (for example, Tektronix CT-1 at 1000 MHz.

Set the simulator charging voltage (Va) to 600 volts. Initiate a simulator pulse and observe the complete current waveform on the oscilloscope. The pulse shall meet the decay time and ringing requirements of Figure 3–1.

Repeat this process for Va = -600 volts. The calibration waveforms must have the characteristics shown in the Notes in Figure 3–1.

3.6.4 PROCEDURE

To ensure reliable results, all devices that undergo ESD testing should first be tested for proper functionally using ATE testing.

Prior to the actual zapping of the device, the I-V characteristics of each pin should be examined using a curve tracer. The part should be powered up to VDD = 5.0 volts when examining the I-V characteristics of each pin. In addition, special care should be taken to limit the current at the onset of junction breakdown. If the current is not limited the junction may become overstressed. The horizontal scale should be set to 5 V division and the vertical scale should be set to 2uA division. Junction breakdown should never be permitted to go beyond 6uA. When observing the I-V characteristics for all data pins, RAS/ and CAS/ should be tied high. The pass/fail criteria is that each pin should be capable of withstanding 7.0 volts of sustained stress and exhibit less than 2uA of leakage at 5.5 volts.

After checking the I-V characteristics of each pin the part is ready to be *zapped*. During *zapping* the part is powered down and all pins except the pin under test should be floating. The actual *zap* consists of 5 discharges with a minimum cool down time of 5 seconds between discharges. In order to ensure the marginality of the ESD protection circuitry, each individual pin should be stressed at -500 V, +500 V, -600 V, +600 V, -700 V and +700 V. Since the Digital specification is 600 V minimum, the results aid in determining the marginality of failures. The test flow is as follows:

1. Check the I-V characteristics of each pin.
2. Zap all pins individually to -500 volts (except VDD and VSS).
3. Check the I-V characteristics of each pin.
4. ZAP all pins individually to +500 volts (except vdd and vss).
5. Check the i-v characteristics of each pin.
6. ZAP all pins individually to -600 volts (except vdd and vss).
7. Check the i-v characteristics of each pin.
8. Zap all pins individually to +600 volts (except VDD and VSS).
9. Check the I-V characteristics of each pin.
10. Zap all pins individually to -700 volts (except VDD and VSS).
11. Check the I-V characteristics of each pin.
12. Zap all pins individually to +700 volts (except VDD and VSS).
13. Check the I-V characteristics of each pin.
14. Test the part on ATE.
15. Zap VDD pin to -600 volts.
16. Zap VDD pin to +600 volts.
17. Test device on ATE.

3.6.5 PASS OR FAIL CRITERIA

All pins should be capable of withstanding the ± 600 volt minimum level. A failure is defined as any pin that exhibits >2uA of leakage at VDD = 0 to 5.5 volts. The test shall be performed on a minimum sample size of 10 devices from at least three separate wafer lots. No failures are permitted.

3.6.6 Summary

All pins must meet the ± 600 volt requirement. Further description of functional testing is found in the Functional Test document.

3.6.7 Reference Document

Refer to *MIL STD 883, Method 3015.7, Electrostatic Discharge Sensitivity Classification*.

ESD DATA (–500 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

ESD DATA (+500 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

ESD DATA (–600 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

ESD DATA (+600 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

ESD DATA (–700 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

ESD DATA (+700 VOLTS)

PIN NUMBER	PIN NAME	SERIAL NUMBER									
		1	2	3	4	5	6	7	8	9	10
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											

3.7 TEST — INPUT AND OUTPUT CAPACITANCE

3.7.1 PURPOSE

This test determines the amount of input and output capacitance between each of the individual clocking signals and VSS, address pins and VSS, as well as Data In and Out and VSS.

3.7.2 EQUIPMENT

1. Two, +5 volt, power supplies
2. Capacitor bridge
3. Textool socket or equivalent

3.7.3 SETUP

Connect the positive terminal of power supply number 1 to the VDD pin of the textool socket. The ground terminal of power supply number 1 is then connected to the VSS pin of the socket. All remaining pins should then be tied to ground except the pin under test. With the capacitor bridge connected to the pin under test and VSS, close the textool socket and zero the bridge. Note that the meter is *zeroed* without a device in the actual socket.

3.7.4 PROCEDURE

Insert the device into the textool socket and turn on power supply number 1 to 5 volts. Record the capacitance measurement between the pin under test and VSS. As previously mentioned, when performing the actual measurement, all remaining pins except for VDD and the pin under test should be tied to VSS. Repeat this procedure for all pins except Data Out, making sure that the test site is *zeroed* for each new pin to be tested using the procedure defined in Chapter 3.

In order to measure the capacitance for Data Out; the positive terminal of power supply number 1 should be connected to the VDD pin of the socket while the ground of power supply should be connected to the VSS pin of the socket. Power supply number 1 should be adjusted to 5.0 volts. Connect the positive terminal of power supply number 2 to RAS/ and CAS/ and adjust the voltage to 2.4 volts. Note that both power supplies 1 and 2 should have a common ground. Make sure that the test site is grounded using the procedure mentioned in Chapter 3. Insert the part and turn on the power supplies. Measure the capacitance between Data Out and VSS.

3.7.5 SUMMARY

The data should be summarized in the accompanying form.

CAPACITANCE DATA

VDD = 5.0 VOLTS, F = 1 MHz

PIN NUMBER	PIN NAME	SERIAL NUMBER										
		1	2	3	4	5	6	7	8	9	10	11
1												
2												
3												
4												
5												
6												
7												
8												
9												
10												
11												
12												
13												
14												
15												
16												
17												
18												
19												
20												

3.8 TEST — LATCH-UP IMMUNITY

3.8.1 PURPOSE

The purpose of this test is to determine the Latch-Up immunity of the power supply pin of the device. This test is only performed on CMOS technology devices.

3.8.2 EQUIPMENT

- Power supply
- Curve tracer
- Textool socket or equivalent

3.8.3 SETUP

All pins of the socket should be tied together; with the exception of VDD, VSS, Data In and Data Out; and connected to the positive terminal of the power supply. The ground terminal of the power supply is then connected to the VSS pin. The Data In and Data Out pins should be left floating. Adjust the power supply to 5.0 volts.

The curve tracer should be used in order to provide a ramped voltage with respect to ground to the VDD pin. Additionally, the curve tracer is used to monitor the current-voltage characteristics of the VDD pin during actual test.

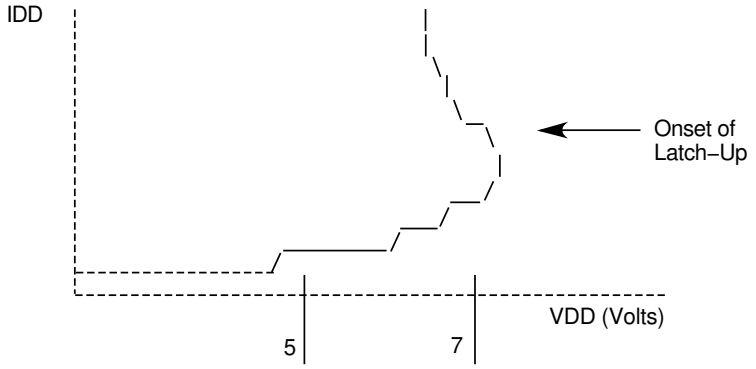
3.8.4 PROCEDURE

Insert the device into the socket and turn on the power supply. With the curve tracer connected to the VDD pin, slowly ramp the voltage from 0 volts to 8.0 volts (see Figure 3.2). Monitor the standby power supply current using the curve tracer.

3.8.5 PASS OR FAIL CRITERIA

Any device that exhibits the the onset of latch-up at or before VDD = 7.0 V, as shown in Figure 3–2, shall be considered a failure. Note junction breakdown may occur between 7 V and 8 V. Occurrence of junction breakdown in this area does not constitute failure. However, concern must be given to the 7.0 V sustained voltage specification. The test shall be performed on a 22-piece sample comprised of a minimum of 3-wafer lots. No rejects shall be permitted.

Figure 3–2: Onset of Latch-Up



LATCH–UP DATA

SERIAL NUMBER	PASS / FAIL	COMMENTS
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		

CHAPTER 4

DRAM QUALIFICATION MECHANICAL/ENVIRONMENTAL TEST PROCEDURES

4.1 TEST—PHYSICAL DIMENSIONS

Procedure	Use the optical measurement system to measure all package dimensions specified for the particular package type under test. The measured readings shall be checked against minimum and maximum limits given by the Digital DRAM packaging specification. Reference Documents: A-PS-2100006-GS *DRAM General Quality Purchase Specification* A-PS-2100008-GS *DRAM General Packaging Specification*
Minimum Sample Size	11
Accept Number	0
Reject Criteria	The device shall be considered a failure if any measurement is out of the specified limits for that package.
VAQ/VSQ Data Required	Using the appropriate table and diagram provided herein, the vendor will make the specified measurements on 11 samples from at least three different date codes, using their own measuring apparatus. The measurements will te tabulated and submitted to Digital along with the samples.

Table 4–1: 16, 19/20, 28-Pin ZIP Package—Vendor Data

PHYSICAL DIMENSIONS TABLES FOR VENDOR–ASSISTED QUALIFICATION

Dim	Min (Vendor Spec)	Max (Vendor Spec)	Actual Measurements										
			1	2	3	4	5	6	7	8	9	10	11
A													
B													
C													
D													
E													
F													
G													
H *													
I													

* Noncumulative

Figure 4–1: 16, 19/20, 28-Pin ZIP Package

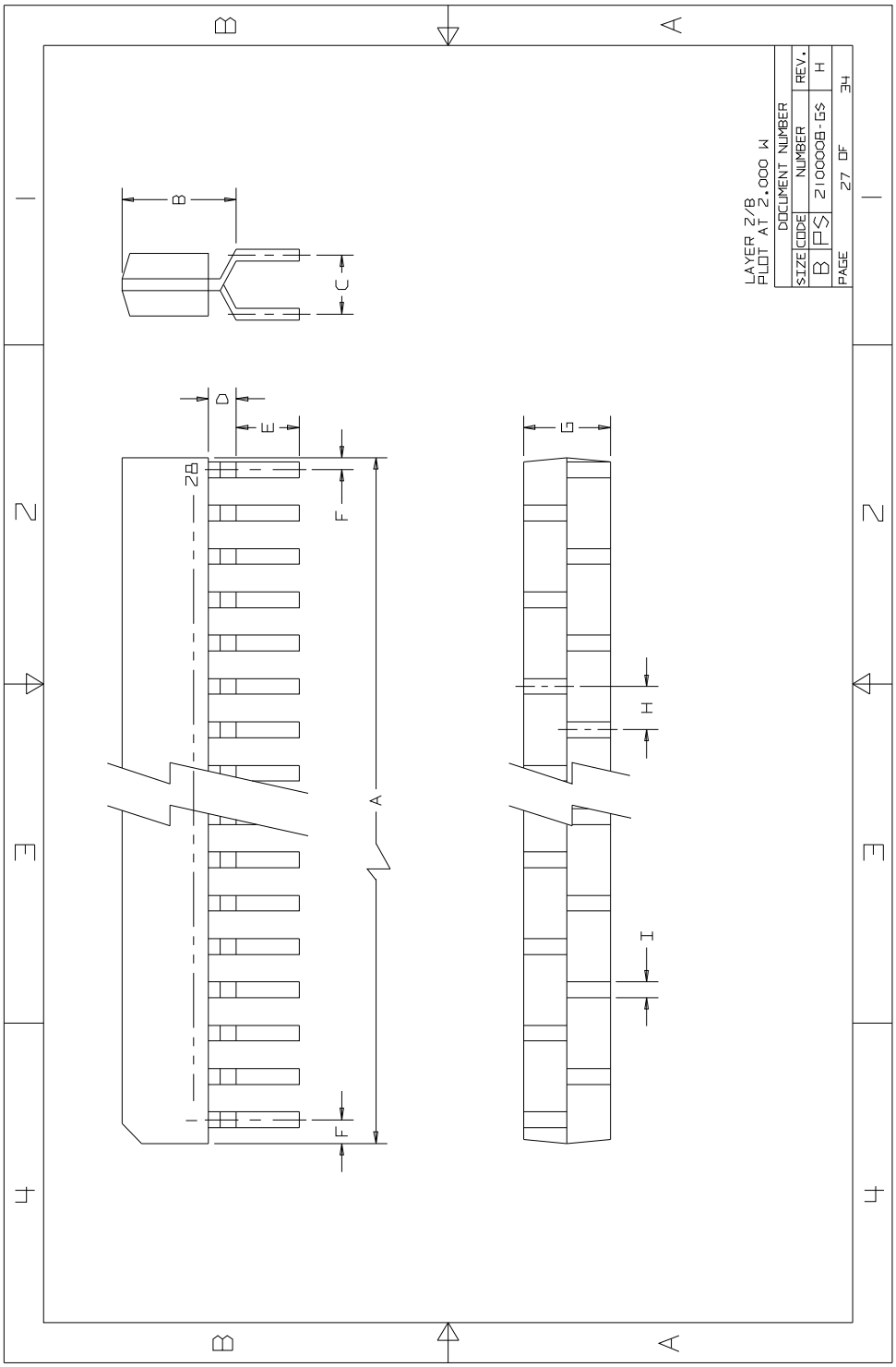


Table 4–2: 16/18-Pin DIP Package—Vendor Data

PHYSICAL DIMENSIONS TABLES FOR VENDOR–ASSISTED QUALIFICATION

Dim	Min (Vendor Spec)	Max (Vendor Spec)	Actual Measurements 1	2	3	4	5	6	7	8	9	10	11
A													
B													
C													
D													
E													
F													
G													
H													
I													
J													
K													
L													
M													
N													
O													
P													

Figure 4–2: 16/18-Pin DIP Package

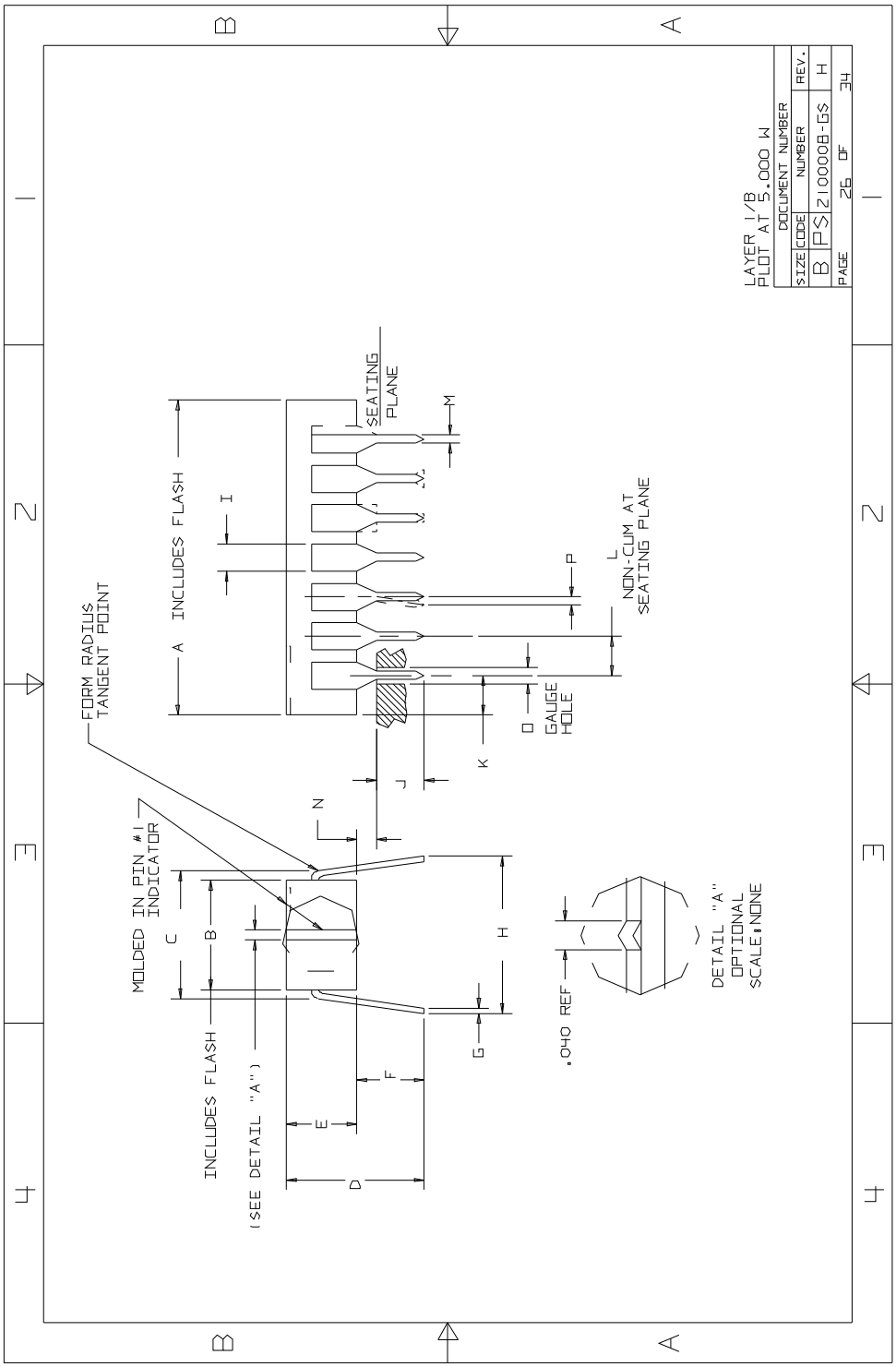


Table 4–3: 18-Pin CLCC Package—Vendor Data

PHYSICAL DIMENSIONS TABLES FOR VENDOR–ASSISTED QUALIFICATION

Dim	Min (Vendor Spec)	Max	Actual Measurements										
			1	2	3	4	5	6	7	8	9	10	11
A													
B													
C													
D													
E													
F													
G													
H													
I													
J													
K													
L													
M													
N													

Figure 4–3: 18-Pin CLCC Package

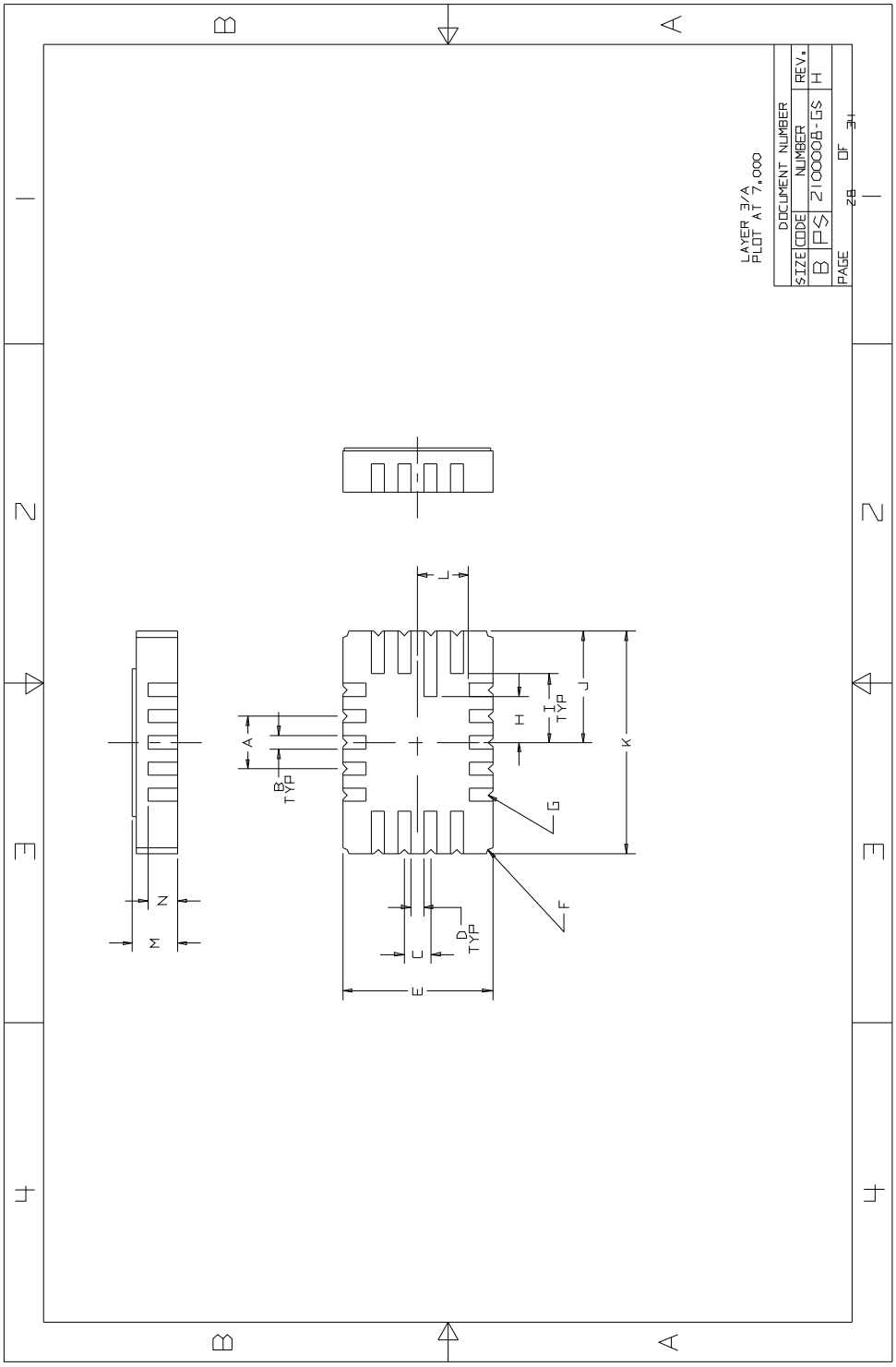


Table 4–4: 18-Pin PLCC Package—Vendor Data

PHYSICAL DIMENSIONS TABLES FOR VENDOR–ASSISTED QUALIFICATION

Dim	Min (Vendor Spec)	Max (Vendor Spec)	Actual Measurements 1	2	3	4	5	6	7	8	9	10	11
A													
B													
C													
D													
E													
F													
G													
H													
I													
J													
K													
L													
M													
N													
O													

Figure 4–4: 18-Pin PLCC Package

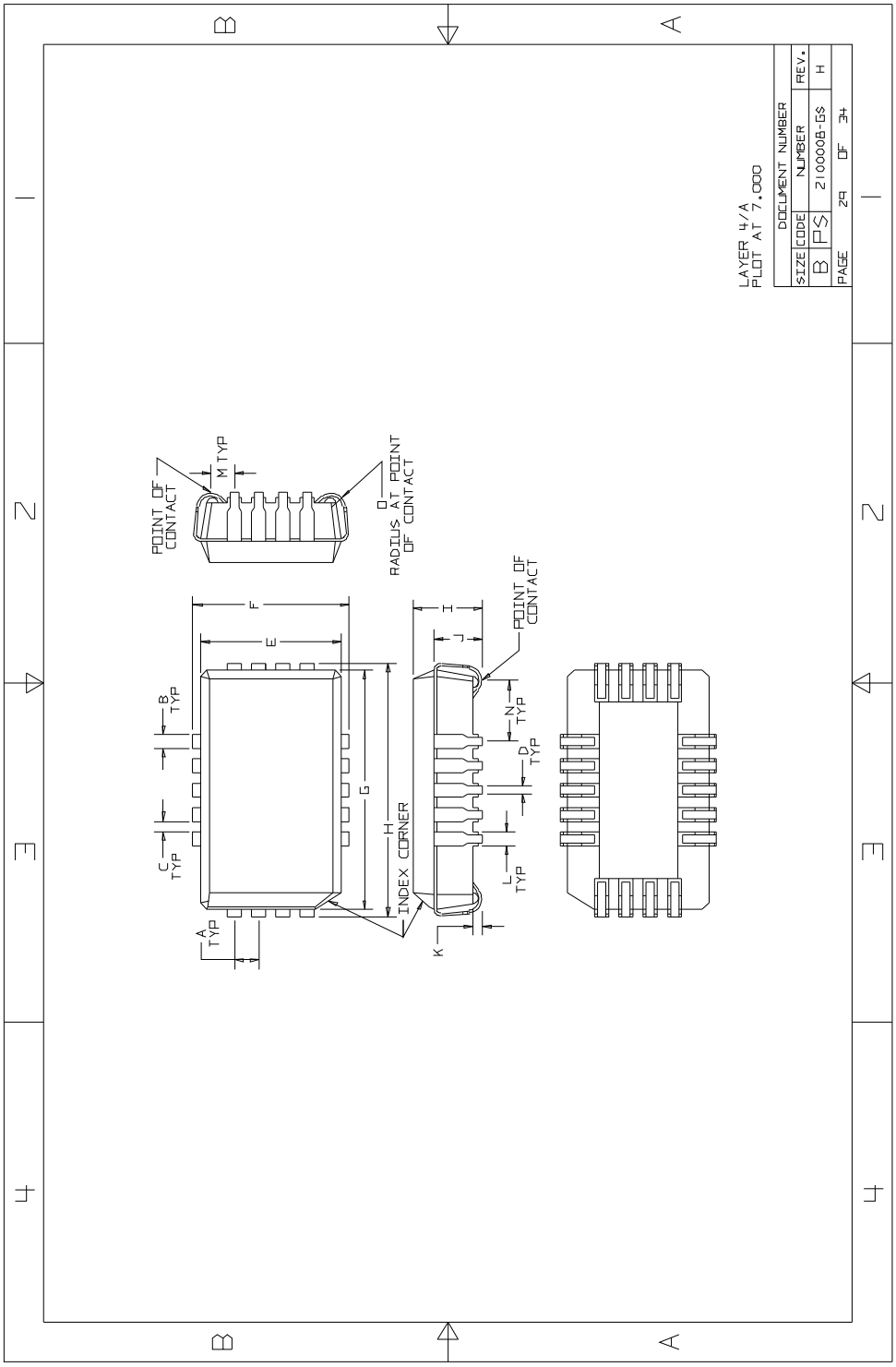


Table 4–5: 20-Pin SOJ Package—Vendor Data

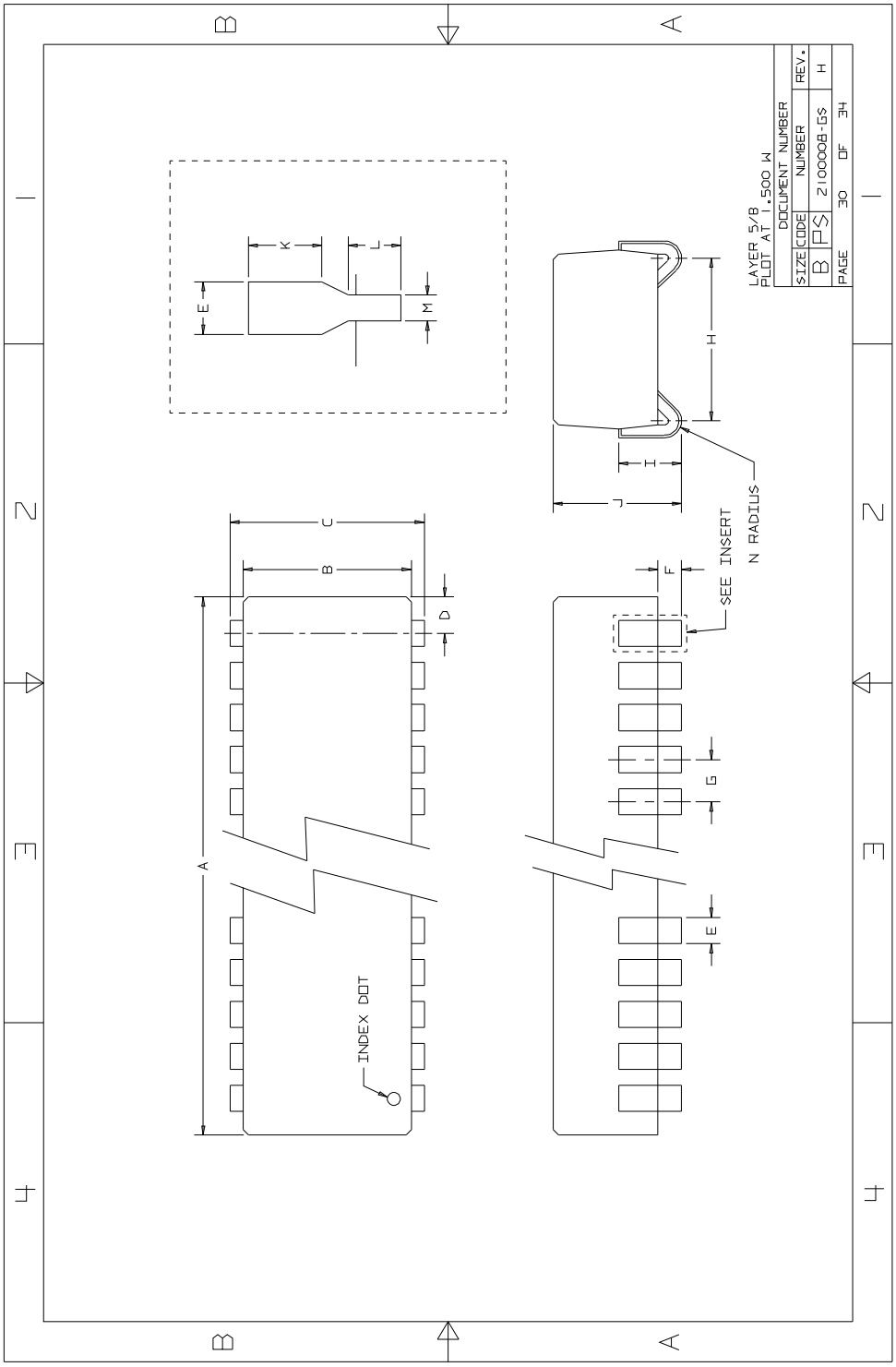
PHYSICAL DIMENSIONS TABLES FOR VENDOR–ASSISTED QUALIFICATION

Dim	Min (Vendor Spec)	Max (Vendor Spec)	Actual Measurements 1	2	3	4	5	6	7	8	9	10	11
A[1]													
B													
C													
D													
E													
F													
G[2]													
H[3]													
I													
J													
K													
L													
M													
N[4]													

Notes

1. Including molding protrusion
2. Noncumulalive at seating plane.
3. Determined at point of contact.
4. Radius at point of contact.

Figure 4–5: 20-Pin, 28-Pin, 40-Pin SOJ Package



4.2 TEST—SOLDERABILITY

Procedure	For SMT devices: steam age for a minimum of 6 hours, apply an appropriate solder paste to leads and expose to 215°C for 30 to 40 seconds. For Non-SMT devices: steam age for a minimum of 6 hours, then dip leads of entire sample size into an appropriate Alpha Flux, then into an appropriate Alpha Solder at 260°C for 5 to 10 seconds. Reference Documents: A-PS-2100008-GS *DRAM General Packaging Specification* MIL STD 883, Method 2003 *Solderability*
Minimum Sample Size	45
Accept Number	0
Reject Criteria	See MIL STD 883, Method 2003 *Solderability*
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 2003 *Solderability*, or supply details of their own internal test method and their test results.

4.3 TEST—LEAD INTEGRITY

Procedure	The devices shall be subjected to the following tests as outlined in the reference document. A. Test condition A —Lead Tension B. Test condition B2—Lead Fatigue C. Test condition C1—Lead Torque Reference Document: MIL-STD-883 Method 2004 *Lead Integrity*.
Minimum Sample Size	11
Accept Number	0
Reject Criteria	See MIL-STD-883, Method 2004 *Lead Integrity*
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 2004 *Lead Integrity*, test conditions A, B2 and C1 or, supply details of their own internal test method and their test results.

4.4 TEST—AUTOCLAVE

Procedure	Devices shall be exposed to 121°C ambient, 100% r.h. and 2 Atm pressure for 96 hours. The devices will be electrically tested before and after the stress. Reference Document: A-PS-2100006-GS *DRAM General Quality Purchase Specification*
Minimum Sample Size	105
Accept Number	2
Reject Criteria	Any device that fails an electrical test at the end of 96 hours shall be considered a reject.
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per the test conditions outlined in the previous procedure or supply their own internal test method and their test results, including any failure analysis that was done.

4.5 TEST—HIGH TEMPERATURE STORAGE

Procedure	Place devices into a chamber (unbiased) at 150°C for 1000 hours. Electrically test at the end of this period. Reference Document: MIL-STD-883 Method 1008 *Stabilization Bake*.
Minimum Sample Size	15
Accept Number	0
Reject Criteria	Any device which fails electrical test at the end of the 1000 hours shall be considered a failure.
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 1008, or supply details of their own internal test method and their test results.

4.6 TEST—X-RAY

Procedure	Take X-ray photos of devices in accordance with reference document. If the X-ray photos show evidence of poor die attach coverage, the component engineer may elect to perform a Lead Frame Peel test. Also check for good wire dress. Reference Document: MIL-STD-883, Method 2012 *Radiography*.
Minimum Sample Size	11
Accept Number	0
Reject Criteria	See MIL-STD-883 Method 2012 *Radiography*
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 2012 *Radiography*, or supply details of their own internal test method and their test results.

4.7 TEST—VISUAL INSPECTION

Procedure	Examine devices and accompanying documentation to insure that the criteria outlined by Reject Criteria segment is met. Devices shall be further examined for lead plating, resin flash on lead, and scratches on leads. Reference Documents: A-PS-2100006-GS *DRAM General Quality Purchase Specification* MIL-STD-883 Method 2009 *External Visual*
Minimum Sample Size	11
Accept Number	0
Reject Criteria	Any device that does not meet Material and Finish, Marking, and Workmanship requirements as specified in the A-PS-2100006-GS *DRAM General Quality Purchase Specification* shall be considered a reject. Also, the criteria outlined in MIL-STD-883 Method 2009.7 *External Visual*, Sections 3.2 a,b,c,g,h.
VAQ/VSQ Data Required	The vendor will supply Digital with the Quality Control (QC) document specifying their visual inspection monitoring process in their assembly and test facility.

MARKING PERMANENCE/MARKING LEGIBILITY TEST PROCEDURE FOR INK AND LASER (RESPECTIVELY) MARKED INTEGRATED CIRCUIT MEMORIES:

4.8 TEST—MARKING TEST PROCEDURE FOR INK AND LASER MARKED ICs

4.8.1 PURPOSE

To verify the permanence of the marking applied to DRAMS and to verify compatibility with aqueous cleaning process.

4.8.2 REFERENCE

Digital document A-SP-ELCE059-TM-002C *Test Method: Marking Permanence.*

4.8.3 EQUIPMENTS AND MATERIALS

The following is a list of the equipment and materials used in marking test.

- Tap water and pressurized water upto a maximum of 450 PSI
- Detergent. Test may be performed with any one of the following or an equivalent detergent approved by Digital.

49-10376-00	Kenco alloy 2230 aquawash
49-01372-00	Hi-grade alloy 7 bio-cleaner (kester 5779)
49-01377-00	London chemical loncoterge, number 520
49-01368-00	Alpha metals 2100

- Safety breakers, 3000ML.
- Hot plate with stirrer.
- Wire mesh basket.
- Thermometer, model 2160A or equivalent.
- Timer with minutes and seconds.
- Drying oven.
- Tweezers or tongs.
- soft cleaning brush.
- Vented fume hood and safety glasses.
- ESD finger cots

4.8.4 SAMPLE SIZE

Eleven devices are used as samples in this testing.

4.8.5 PROCEDURE

The procedure for the marking test is as follows.

1. Mix a solution consisting of 93% water and 7% detergent (95% water and 5% detergent for 49-01368-00 and 49-01377-00). It must fill at least one half of a breaker. Stir the solution thoroughly. Use a new solution every two hours, or if contaminated by bad devices.
2. Place the beaker containing the solution on a heated hot plate. Maintain temperature between 145°F and 150°F (62.8°C and 65.6°C). Use the magnetic stirrer to agitate the mixture.
3. Turn on drying oven and set oven temperature to 202°F (94.4°C)
4. Immerse the test devices into the solution for (10) seconds. Use the timer to measure the immersion time. Use ESD finger cots when handling ICs.
5. Rinse the devices with pressurized warm water for a period of (1) minute. The max water pressure not to exceed 450 PSI and the temperature of water to be between 20°C and 35°C.
6. Dry the devices for 15 minutes in the heated oven.
7. Allow the devices to recover to room temperature, then lightly brush the component marking (4) times, after having dipped the brush once into tap water at room temperature (twice in each direction)
8. Dry the devices for 15 minutes in the heated oven to ensure that the devices are dry.

4.8.6 REJECT CRITERIA

To test for rejection of a device, follow these steps.

1. Inspect the tested devices for marking degradation such as smearing, discoloration or running. Any degradation is considered a failure and indicates lot rejection. All device marking must be legible.
2. Reference sample tables
3. Inspect cleaning solution at the end of each test to insure no gross foreign contaminants are coming off the test devices.
4. Record results, initial and date LTF.

4.9 TEST—PLATING ANALYSIS

Procedure	Examine cross-section leads in both vertical and horizontal orientations and measure thickness of lead plating using mutually agreed upon techniques. Tin/lead composition shall also be determined using mutually agreed upon techniques. Reference Documents: A-PS-2100006-GS *DRAM General Quality Purchase Specification* A-PS-21-00008-GS *DRAM General Packaging Specification*
Minimum Sample Size	22
Accept Number	0
Reject Criteria	As in A-PS-2100006-GS *DRAM General Quality Purchase Specification* and A-PS-2100008-GS *DRAM General Packaging Specification*
VAQ/VSQ Data Required	The vendor will supply Digital with the following information: - Statement of composition of lead frame material - Details of the process used for measuring lead-plating thickness, and the data collected on the subject qualification using this process.

4.10 TEST—TEMPERATURE CYCLING

Procedure	The unbiased devices shall be cycled between 2 temperature zones of 150° (+15°,-0°)C and -65° (+0°,-10°)C for the following number of cycles: 50 for ceramic packages and 100 for plastic packages. The time in each zone at temperature shall be a minimum of 10 minutes. Reference Documents: MIL-STD-883, Method 1010 *Temperature Cycling* A-PS-2100006-GS *DRAM General Quality Purchase Specification*
Minimum Sample Size	15
Accept Number	0
Reject Criteria	See MIL-STD-883, Method 1010 *Temperature Cycling*
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 1010 *Temperature Cycling*, or supply details of their own internal test method and their test results.

4.11 TEST—THERMAL SHOCK

Procedure	Devices shall be exposed to (fifty) 5-minute cycles of immersion in -65° to 150°C liquid baths. Reference Documents: MIL STD 883, Method 1011 *Thermal Shock* Condition C A-PS-2100006-GS *DRAM General Quality Purchase Specification*
Minimum Sample Size	11
Accept Number	0
Reject Criteria	Any device that fails electrical or visual test at the end of the 50 cycles shall be considered a reject. See MIL-STD-883, Method 1011 *Thermal Shock* .
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 1011 *Thermal Shock*, Condition C, or supply details of their own internal test method and their test results.

4.12 TEST—85/85

Procedure	Place electrically tested good devices in socketed boards with device pins alternately biased to 5.0 V and ground. Plug the boards into the powered backplane of a test chamber that will be brought up to and maintained at 85°C and 85% relative humidity. After 1000 hours (6 weeks) remove the devices and electrically test.
Minimum Sample Size	105
Accept Number	2
Reject Criteria	A device that is determined to be a hard electrical test failure shall be considered a reject. It may be necessary to bake initial failures at 150°C for up to 10 days in order to determine if the failures are hard.
VAQ/VSQ Data Required	The vendor will supply Digital with their test process for this test, along with their test data collected on the part under VSQ qualification.

4.13 TEST—HAST

Procedure	Place devices in socketed boards with device pins alternately biased to 5.0 volts, and ground. Plug the boards into the powered backplane of a test chamber that will be brought up to and maintained at 125°C and 85% relative humidity. After 100 hours, remove the devices and place in 150°C oven unbiased for 48 hours. After this baking, remove the devices and electrically retest. Reference Document: None at this time.
Minimum Sample Size	105
Accept Number	2
Reject Criteria	A device that is found to be a hard electrical test failure shall be considered a reject. It may be necessary to bake initial failures at 150°C for up to 10 days in order to determine if the failures are hard.
VAQ/VSQ Data Required	The vendor will supply Digital with their test process for this test, along with their test data collected on the part under requalification.

4.14 TEST—MECHANICAL SHOCK

Procedure	Using appropriate apparatus, subject devices to five shock pulses of 1500 g peak in each of the specified device orientations. Reference Document: MIL-STD-883, Method 2002 *Mechanical Shock* Test Condition B.
Minimum Sample Size	11
Accept Number	0
Reject Criteria	Per MIL-STD-883, Method 2002 *Mechanical Shock*
VAQ/VSQ Data Required	The vendor will supply Digital with the results of their testing per MIL STD 883 Method 2002 *Mechanical Shock*, Condition B, or supply details of their own internal test method and their test results.

4.15 TEST—DIE PHOTO

Procedure	After decapsulating the device, a color photograph shall be taken of die, showing all markings (revision, mask layers, vendor logo, and so on.) Two copies of the photo will be made. One copy will go into the file for qualification, the other goes to the Manufacturing Group for use at incoming inspection. Reference Documents: A-PS-2100006-GS *DRAM General Quality Purchase Specification*
Sample Size	1
Accept Number	NA
Reject Criteria	NA
VAQ/VSQ Data Required	The vendor shall supply Digital with: • An 8 x 10-inch color photo of the die being qualified. • Close up photos of all die markings. • A statement from the vendor specifying the marking that will be on the package body to denote the revision of the die.

4.16 TEST—COPLANARITY

Procedure	After mounting device, optically measure the coplanarity of the leads, which is the distance between any lead contact point and the seating plane, in a direction perpendicular to the seating plane. Reference Document: A-PS-2100008-GS *DRAM General Packaging Specification*
Minimum Sample Size	76
Accept Number	0
Reject Criteria	Per A-PS-2100008-GS *DRAM General Packaging Specification*
VAQ/VSQ Data Required	The vendor will supply Digital with their test process for determining compliance to specification of coplanarity of surface-mounted packaged devices.

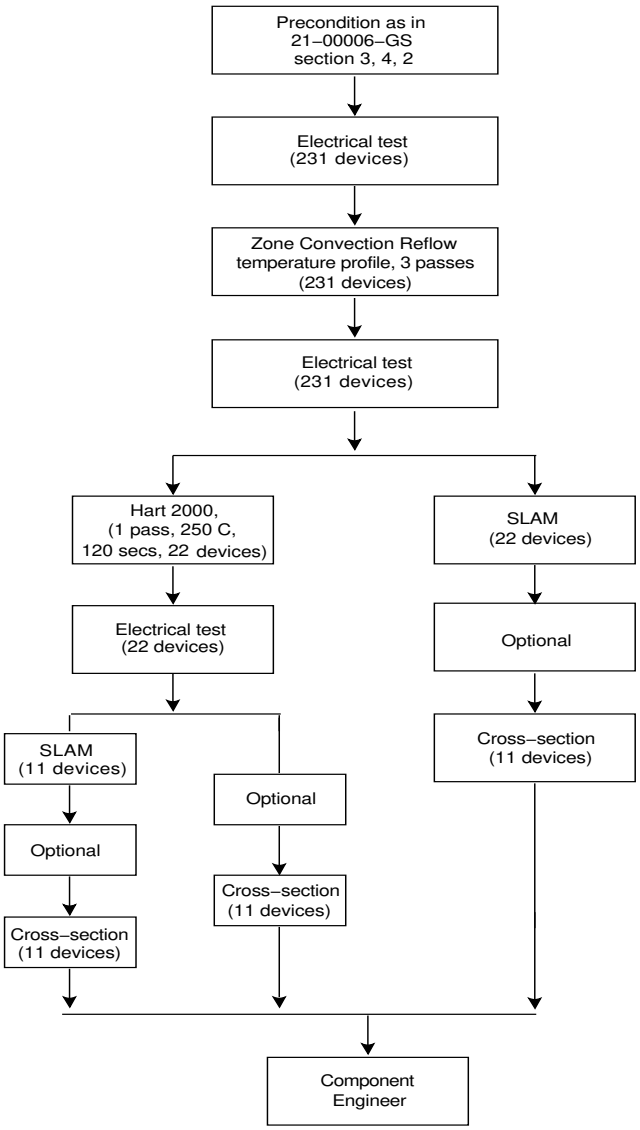
4.17 TEST—PLATING ADHESION

Procedure	Using an xacto knife, score the surface of the flat portion of the exposed lead in the shape of a square or rectangle. Make the length and width of the square or rectangle proportional to the length and width of the flat portion of the lead. The depth of the score must be at least the depth of the solder plating to the metal lead frame. Do this for half the total number of pins on the device. Place a strip of Scotch tape number 540, 640 or 810 across the leads, totally covering the scored areas. Press firmly with fingertips to insure good contact. Then, peel the tape off the leads quickly. Examine the leads of the devices under a microscope to determine if any of the lead plating was removed by the tape. Reference Document: 1986 Semi Standard for Packaging, Vol. 4 (At the discretion of the responsible component engineer, MIL-STD-883, Method 2025 *Adhesion Of Lead Finish*, may be used in place of, or in addition to this test.)
Minimum Sample Size	5
Accept Number	0
Reject Criteria	If any plating is removed by the tape, the device shall be rejected.
VAQ/VSQ Data Required	The vendor will supply Digital with their test process for determining compliance of lead-plating adhesion to specification, along with their test data collected on the part under VSQ qualification.

4.18 TEST—PROCESS COMPATIBILITY

Procedure	After 3 passes of IR preheat and zone convection reflow (ZCR) conditions, devices shall be exposed to 250°C hot air for 120 seconds (see flowchart following). Reference Documents: A-PS-2100006-GS *DRAM General Quality Purchase Specification*

PROCESS COMPATIBILITY FLOW



Note

1. SLAM: Detects die and package cracks, and delamination.
2. Cross section: Detects die and package cracks.
3. Electrical test: Verifies that the ac and dc characteristics meet specifications.

CONDITIONS FOR ZONE CONVECTION REFLOW

PARAMETER	TEST CONDITION
Max. temperature at reflow	225°C
Min. temperature at reflow	205°C
Max. duration at or above 183°C (liquidus)	90 seconds
Max. temperature ramp (delta-T) during Vapor Phase	2°C/seconds
Max. time above 150°C	330 seconds

The module may see as many as 3 reflow temperature profiles.

NOTE

The above conditions may or may not be present simultaneously, for example, during the same Prebake/Vapor Phase pass.

Minimum Sample Size	231
Accept Number	0
Reject Criteria	Any device that fails electrically or mechanically at any point of the flow shall be considered a reject. Mechanical failures shall be detected using both scanning laser acoustic microscopy (SLAM) and package cross-sectional techniques, including the following: – Any die cracks – Any major die delaminations that may negatively impact reliability as determined by the responsible component engineer – Any package cracks that propagate to the exterior of the package Any devices with minor die delaminations or package cracks that do not propagate to the exterior of the package will be analyzed more thoroughly, that is exposed to additional thermal and mechanical stresses.
VAQ/VSQ Data Required	The vendor will supply to Digital their test process for determining the ability of the part to withstand the reflow portion of manufacturing process. The vendor will also supply the data they have collected using this test process.

CHAPTER 5

DRAM REQUALIFICATION RELIABILITY TEST PROCEDURES

5.1 TEST—SOFT ERROR RATE TESTING

5.1.1 PURPOSE

This document describes the requirements and procedures that are to be used as a guideline for determining the soft error rate for dynamic RAMs. This test is to be conducted as a system level test on a large sample of devices that are operated under the constraints of the purchase specification.

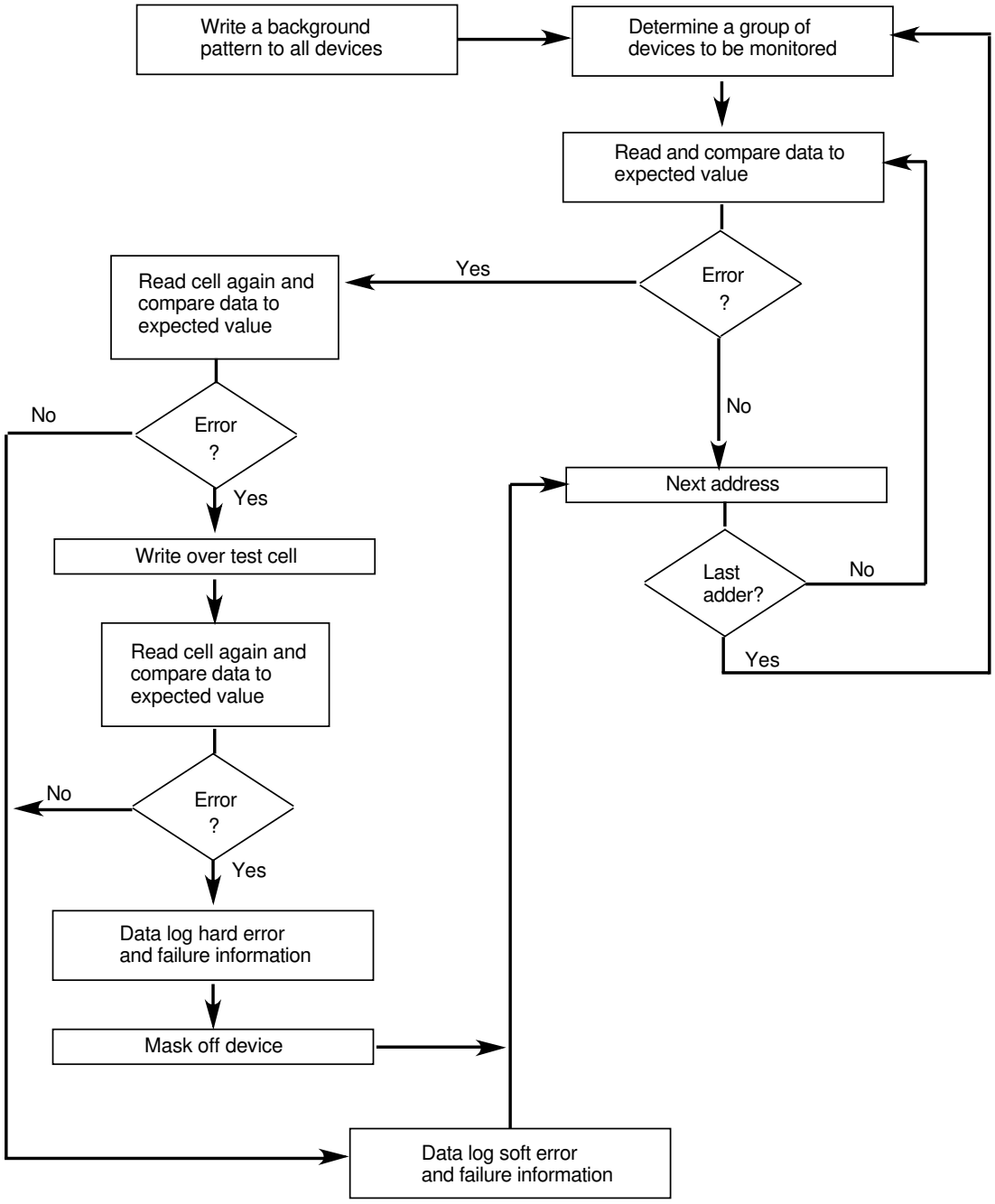
5.1.2 REQUIREMENTS

A minimum of 1000 devices equally represented from at least three wafer/package lots shall undergo system level testing for a minimum of 1,000,000 device hours. System level testing is defined as continuous parallel testing of all parts to read, write, and refresh operations per the constraints of the device purchase specification. System level testing shall be performed at max Ta and Vdd = minimum. Read/write operations should be performed with a maximum cycle rate of 1 microsecond.

5.1.3 TEST SYSTEM FLOW

Figure 5–1 shows a flowchart outlining the general implementation for system level soft error testing; checkerboard and inverted checkerboard patterns are used.

Figure 5–1: System Level Soft Error Testing Flowchart



5.1.4 PASS OR FAIL CRITERIA

The maximum allowable soft error rates are defined in A-PS-21-00006-GS, Section 3.3.2.2. A FIT is defined as failures in time where time is taken to be 1-billion device hours. Therefore, for a 1-megabit device, the allowable failure rate is defined as 10,000 soft errors maximum allowable within 1-billion device hours. The maximum allowable soft error rate for 256K devices is 1,000 FITs. The failure rate shall be calculated at a 60% confidence level and based on a minimum of 1-million device hours.

5.1.5 DATA

The supplier shall provide the following information:

Number of parts tested: _____

Duration of time on system level test: _____

Temperature: _____

Operating power supply voltage: _____

Cycle rate: _____

Number of soft errors: _____

Number of hard failures: _____

5.2 TEST—HOT CARRIER TEST

5.2.1 PURPOSE

Hot Carrier testing determines the degradation of device performance as a result of high energy carriers traversing the channel region.

5.2.2 PROCEDURE

A minimum of 22 devices from at least 3 different wafer lots shall be exercised dynamically for 1000 hours at VDD = maximum and -10°C. Prior to subjecting the devices to Hot Carrier testing, all devices should be fully characterized at min/max Ta with a measurement system having adequate accuracy and resolution. Characterization parameters, as a minimum, include the following:

— VIL (All pins)
— VIH (All pins)
— VOL (Data out)
— VOH (Data out)
— tRAC
— tCAC
— VDD minimum operating
— VDD maximum operating
— tREFRESH (RAS/ only refresh, burst)

— tREFRESH (RAS/ only refresh, distributed)

— tREFRESH (CAS/ before RAS/ refresh, burst)

— tREFRESH (CAS/ before RAS/ refresh, distributed)

All devices should be fully characterized at time equals 0 hours, 500 hours, and 1000 hours. Dynamic stress testing should include read, write, and refresh operations per the purchase specification. The cycle rate should be less than 2 microseconds.

5.2.3 CONTROLS

In order to accurately note parametric shifts in device performance, the use of controls shall be employed. As a minimum, five control devices should be used. The five control devices shall be tested, along with the devices that are subjected to Hot carrier Testing, at each of the three read points (0 hour, 500 hours, and 1000 hours). The controls shall not be stressed in any manner, and therefore will aid in determining the amount of drift in test values that may occur over time as a result of either tester calibration or accuracy.

5.2.4 REQUIRED DATA

The raw data for each part shall be tabulated in Tables 5-1 through 5-12. Each table has two sections, A and B; the contents are described in this section. At each of required read points, the control samples shall be characterized at max Ta. The average values for each parameter shall then be computed using the data from the 5-piece control sample. These average values shall be used as the basis for obtaining normalized parametric values. Normalized data does not need to be computed for initial testing at time zero. To normalize the test data at 500 and 1000 hours, use the following equation:

Let,

D(parameter/0) = average parameter value of the control samples tested at time zero

NOTE: D(VIL/0) = average value of VIL obtained using the control samples at time = 0 hours

S(parameter/hours) = value of the parameter to be normalized at either 500 or 1000 hours

NOTE: S(VIL/1000) = value of VIL at 1000 hours to be normalized

N(parameter/time) = normalized value at either 500 or 1000 hours

NOTE: N(VIL/1000) = normalized value of VIL at 1000 hours

$$N(\text{parameter/hours}) = \frac{S(\text{parameter/hours}) * D(\text{parameter/0})}{D(\text{parameter/hours})}$$

Data for each parameter should be recorded in two tables: 5-1A and 5-2B. Table 5-1A is used to record the actual tested values for each device at 0, 500, and 1000 hours. The column for Normalized Data is used to record the worst-case normalized shift in values that occurs over time. The delta should be calculated in terms of a percentage value. To calculate the Normalized Delta for each parameter or part; use EQ(1) and solve for N(parameter/500 hours) and N(parameter/1000 hours). Next, solve for:

$$\left[1 - \frac{\text{S(parameter/0 hours)}}{\text{N(parameter/500 hours)}}\right] * 100 \quad \text{and} \quad \left[1 - \frac{\text{S(parameter/0 hours)}}{\text{N(parameter/1000 hours)}}\right] * 100$$

Enter the greater of the two values in the Normalized Data column.

Table 5-1B is used to record the mean values for the control sample and the Hot Carrier Sample at each of the read points. The normalized values are determined in the same manner as mentioned above.

5.2.5 PASS OR FAIL CRITERIA

Any device that shifts over time by greater than 10% of the initial value or exceeds the maximum or minimum limit of the purchase specification is cause for failure. The one exception is access time related parameters. Furthermore, tCAC and tRAC may not exceed 95% of the maximum specified limit. All calculated parametric changes should be based on normalized values.

Table 5–1: VIL (All Pins)

VIL (ALL PINS)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-1: VIL (All Pins) (continued)

VIL (ALL PINS) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–2: VIH (All Pins)

VIH (ALL PINS)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
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16				
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18				
19				
20				
21				
22				

Table 5-2: VIH (All Pins) (continued)

VIH (ALL PINS) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–3: V0L (Data Out)

V0L (DATA OUT)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-3: V0L (Data Out) (continued)

V0L (DATA OUT) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–4: VOH (Data Out)

VOH (DATA OUT)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-4: VOH (Data Out) (continued)

VOH (DATA OUT)
TABLE B

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ
A			
B			
C			
D			
F			
L.T.O.L. SAMPLE			
1			
2			
3			
4			
5			
6			
7			
8			
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20			
21			
22			

Table 5-4: VOH (Data Out) (continued)

VOH (DATA OUT) DATA SUMMARY
TABLE C

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–5: tRAC

tRAC
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
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20				
21				
22				

Table 5-5: tRAC (continued)

tRAC
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–6: tCAC

tCAC
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
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19				
20				
21				
22				

Table 5-6: tCAC (continued)

tCAC
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–7: VDD (Minimum)

VDD (MINIMUM)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
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12				
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14				
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16				
17				
18				
19				
20				
21				
22				

Table 5-7: VDD (Minimum) (continued)

VDD (MINIMUM) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–8: VDD (Maximum)

VDD (MAXIMUM)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
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18				
19				
20				
21				
22				

Table 5-8: VDD (Maximum) (continued)

VDD (MAXIMUM) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–9: tREFRESH (RAS/Only Refresh, Burst)

tREFRESH (RAS/ ONLY REFRESH, BURST)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-9: tREFRESH (RAS/Only Refresh, Burst) (continued)

tREFRESH (RAS/ ONLY REFRESH, BURST) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–10: tREFRESH (RAS/Only Refresh, Distributed)

tREFRESH (RAS/ ONLY REFRESH, DISTRIBUTED)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-10: tREFRESH (RAS/Only Refresh, Distributed) (continued)

tREFRESH (RAS/ ONLY REFRESH, DISTRIBUTED) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–11: tREFRESH (CAS/Before RAS/ Refresh, Burst)

tREFRESH (CAS/ BEFORE RAS/ REFRESH, BURST)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
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12				
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14				
15				
16				
17				
18				
19				
20				
21				
22				

Table 5-11: tREFRESH (CAS/Before RAS/Refresh, Burst) (continued)

tREFRESH (CAS/ BEFORE RAS/ REFRESH, BURST) DATA SUMMARY
TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

Table 5–12: tREFRESH (CAS/Before RAS/Refresh, Distributed)

tREFRESH (CAS/ BEFORE RAS/ REFRESH, DISTRIBUTED)
TABLE A

CONTROL SAMPLE	0 HR READ	500 HR READ	1000 HR READ	NORMALIZED DELTA (%)
A				
B				
C				
D				
F				
L.T.O.L. SAMPLE				
1				
2				
3				
4				
5				
6				
7				
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18				
19				
20				
21				
22				

Table 5-12: tREFRESH (CAS/Before RAS/Refresh, Distributed) (continued)

tREFRESH (CAS/ BEFORE RAS/ REFRESH, DISTRIBUTED) DATA SUMMARY TABLE B

TIME	MEAN VALUES		
	CONTROL SAMPLE	HOT CARRIER SAMPLE	NORMALIZED VALUES
O HR			
500 HR			
1000 HR			
DELTA			

NOTE

Any normalized device that shifts greater than 10% of the original value is considered a failure.

5.3 TEST—ACCELERATED LIFE TEST

Procedure

Shall be done per MIL-STD-883 Method 1016 *Lift/Reliability Characterization Tests*, with the following exceptions. Test duration, sample size, and accept number shall be calculated by the responsible component engineer based on:

1. Activation energy of 0.44 eV
2. Test temperature of 125°C ambient or 140°C junction, whichever yields a higher ambient temperature.
3. Temperature acceleration is calculated as follows:

$$A_t = exp^{(Ea/kT_1 - Ea/kT_2)}$$

where:
A_t = Acceleration factor due to temperature
Ea = Activation energy (eV)
k = Boltzman's constant (8.62×10^{-5})
T_1 = Reference voltage (V) = maximum operating voltage (degrees K)
T_2 = Stress temperature (degrees K)

4. Voltage acceleration for cell oxide failures is given by:

$$Av_1 = exp^{\frac{C(V_1 - V_2)}{Tox_1(n)}}$$

where:
Av_1 = Acceleration factor due to voltage for cell oxide failures
C = Constant (A/V)
Tox_1 = Dielectric thickness of cell capacitor (A)
V_1 = Stress voltage (V)
V_2 = Reference voltage (V) = maximum operating voltage
n = 2 if 1/2 Vcc cell plate design; 1 if full Vcc cell plate design

5. Voltage acceleration for pass transistor oxide failures is given by:

$$Av_2 = \frac{C(V_1 - V_2)B}{Tox_2}$$

where:
Av_2 = Acceleration factor due to voltage for pass transistor oxide failures
B = Factor by which VDD is multiplied to get wordline select voltage
C = Constant (Å/V)
Tox_2 = Pass transistor oxide failure
V_1 = Stress voltage (V)
V_2 = Reference voltage (V) = maximum operating voltage

6. Calculated acceleration factor shall be derated to maximum operating ambient temperature and supply voltage.

	The life test shall be dynamic in nature, that is, the device address pins shall cycle starting from the lowest address going to the highest address performing a read/modify/write sequence of operations on each memory cell. The cycle time of each sequence of operations shall be specified by the component engineer for each device type. The device sample shall be electrically tested at any temperature called out by the purchase specification after the test has completed its duration, to determine if any the number of induced failures. All failures from this test shall be analyzed either at Digital or returned to the supplier. Test results analysis shall include calculation of the hard failure rate per billion device hours (FITs). Reference Documents: MIL-STD-883 Method 1016 *Lift/Reliability Characterization Tests*, A-PS-2100006-GS
Note:	Failure analysis must be done to determine failure mechanism, but at this writing, the majority of single-bit failures are due to pass transistor oxide defects, as in item 5 of this table.
Sample size	Determined by the responsible component engineer. The sample size must be sufficient to allow the FIT calculation to resolve to 50 FITs. Generally, the sample size will not exceed 2000.
Accept number	Determined by the responsible component engineer based on 1 through 4 in the above Procedure.
Reject criteria	Calculated failure rate shall not exceed 500 FITs derated to max Ta and VDD max at 60% confidence level.
VAQ/VSQ data required	Supply the information and data requested below:

5.3.1 OVERVIEW

Digital would like to use vendor High Temperature Operating Life (HTOL) test data to assist in doing DRAM qualifications. To accomplish this qualification, Digital must know the vendor's process for running this test, as well as methods used by the vendor to calculate results.

5.3.2 PURPOSE OF HTOL TESTING AT DIGITAL

1. Check the devices for any gross reliability problem.
2. Measure the effectiveness of the vendor's outgoing burn-in process.
3. Provided the vendor's outgoing burn-in is effective, measure the steady-state failure rate in the early life of the device.

5.3.3 CONDITIONS OF DIGITAL'S HTOL TEST

1. VDD = 7.0 V (for 5 V devices; the stress voltage for 3.3 V devices is TBD)
2. Temperature = 125°C
3. Sample size: 1000 devices
4. Time duration: 216 hours
5. Cycle time = 33 Ons
6. Pattern = CKBD, /CKBD

Digital requests the following information from the vendor to be used doing HTOL testing using a vendor-assisted qualification.

5.3.4 CONDITIONS OF VENDOR'S HTOL TEST

1. VDD = _____
2. Temperature = _____
3. Sample size = _____
4. Time duration = _____
5. Cycle time = _____
6. Pattern = _____
7. Voltage acceleration factor = _____
8. Formula for calculating voltage acceleration factor = _____
9. Activation energy used for determining temperature acceleration factor:
10. Temperature acceleration factor:
11. Temperature acceleration is derated to:
12. Results of vendor HTOL test:

    Number of fails _____
    Vendor calculated failure rate _____
    Analysis of failures
13. Please describe your outgoing burn-in process:
    - 100% BI? Yes No

      If no, describe your sample plan:

    - Burn-in duration _____
    - Temperature _____
    - VDD _____
    - Pattern _____
    - Cycle time _____
    - Percent defective allowed before lot is held for further burn-in or evaluation: _____
    - Predominant failure modes seen in burn-in rejects:

5.4 TEST—MODULE QUALIFICATION

Procedure

Component Engineering and/or Purchasing must inform Manufacturing Engineering of a new device or changes being made to a present device. Component and Manufacturing Engineering will determine if a module qualification is required. If a module qualification is needed, Component and Manufacturing. Engineering will determine the sample size and start and completion dates of the qualification. Manufacturing Engineering is responsible to determine the test conditions, such as test patterns, voltage margins, and temperature at which the modules will be exercised defined by the device purchase specification.

NOTE

Successful completion of this test will not demonstrate compliance with the hard error reliability specification of 500 FITs. This test is intended to assess the general performance of the device in a memory module environment.

Sample size

The exact sample size for a qualification is based on the module used for qualification and the manufacturing. Engineer's confidence level and knowledge of the device under qualification; qualification requires a minimum of 3000 devices and a maximum of 4000 devices.

Reject criteria

200 ppm or less is required for the first complete test cycle. The first test cycle is concluded when the module has been tested through all combinations of patterns, voltage, and temperature. The length of time of this cycle will vary from module to module.

The reject criteria, following this first cycle, is one or more failures, since the resultant failure rate would exceed our hard error specification limit of 500 FITs. This is exclusive of device failures which are considered nonrepetitive (that is, soft error). A nonrepetitive failure will be ignored. Marginal failures will be evaluated to determine if the failure occurred during the first test cycle or subsequent test cycles. If the failure occurs during subsequent test cycles the supplier will determine the nature of the problem and provide a corrective action statement prior to a re-qualification attempt.

Modules will be exercised in thermal cycle for a minimum of 96 hours during the qualification process.

APPENDIX A REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-CE059-TM	*Test Method: Marking Permanence*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

A.2 Other Digital Documents

Document Number	Document Title
A-PS-2100006-GS	*DRAM General Quality Purchase Specification*
A-PS-2100008-GS	*DRAM General Packaging Specification*

A.3 Other Documents

Document Number	Document Title
1986 SEMI STANDARD	*1986 Semi Standard for Packaging, Vol. 4*
MIL STD 883, (1008)	*MIL STD 883, Method 1008; Stabilization Bake*
MIL STD 883, (1010)	*MIL STD 883, Method 1010; Temperature Cycling*
MIL STD 883, (1011)	*MIL STD 883, Method 1011; Thermal Shock*
MIL STD 883, (1016)	*MIL STD 883, Method 1016; Lift/Reliability Characterization Tests*
MIL STD 883, (2002)	*MIL STD 883, Method 2002; Mechanical Shock*
MIL STD 883, (2003)	*MIL STD 883, Method 2003; Solderability*
MIL STD 883, (2004)	*MIL STD 883, Method 2004; Lead Integrity*
MIL STD 883, (2008)	*MIL STD 883, Method 2008; Visual and Mechanical*
MIL STD 883, (2009)	*MIL STD 883, Method 2009; External Visual*
MIL STD 883, (2012)	*MIL STD 883, Method 2012; Radiography*
MIL STD 883, (2025)	*MIL STD 883, Method 2025; Adhesion Of Lead Finish*
MIL STD 883,(2009.7)	*MIL STD 883, Method 2009.7; External Visual*
MIL STD 883,(3015.7)	*MIL STD 883, Method 3015.7; Electrostatic Discharge Sensitivity Classification*

A.4 Ordering Information

Following are the sources for documents not available from Standards and Methods Control.

- Federal Standards, Military Standards, Naval Publications, and Forms Center:
  5801 Tabor Avenue
  Philadelphia, PA 19120
  Telephone (215) 697-3321
- Central Specification Control Systems
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